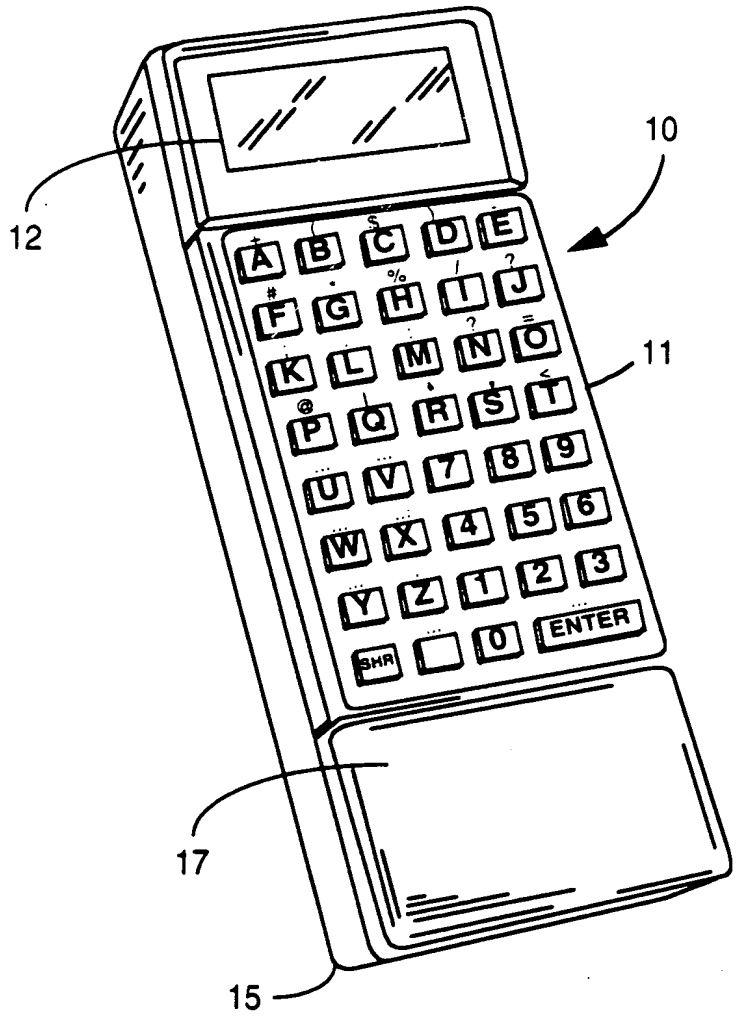

12
10
11
17
15
A B C D E
F G H I J
K L M N O
P Q R S T
U V 7 8 9
W X 4 5 6
Y Z 1 2 3
SHR 0 ENTER

FIG. 1

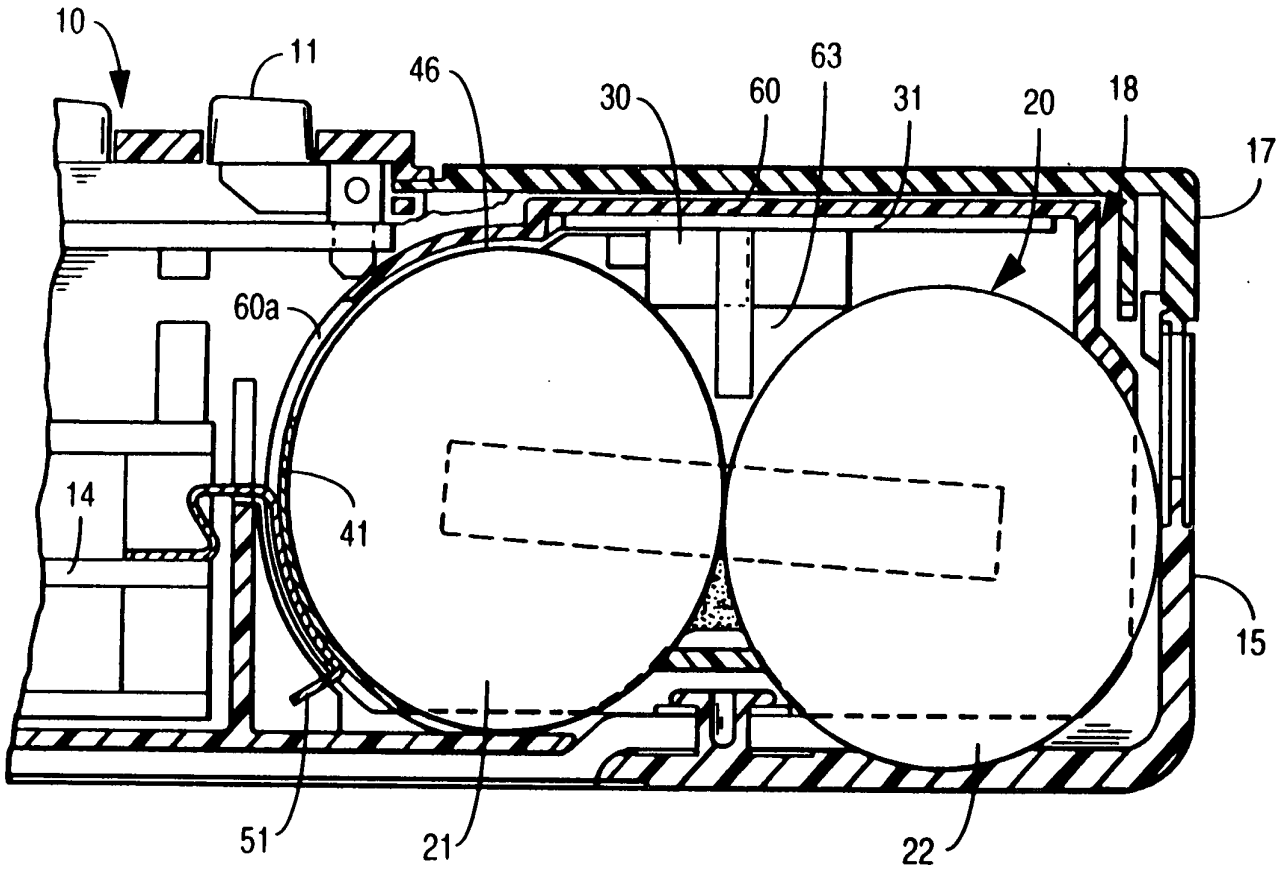


FIG. 2

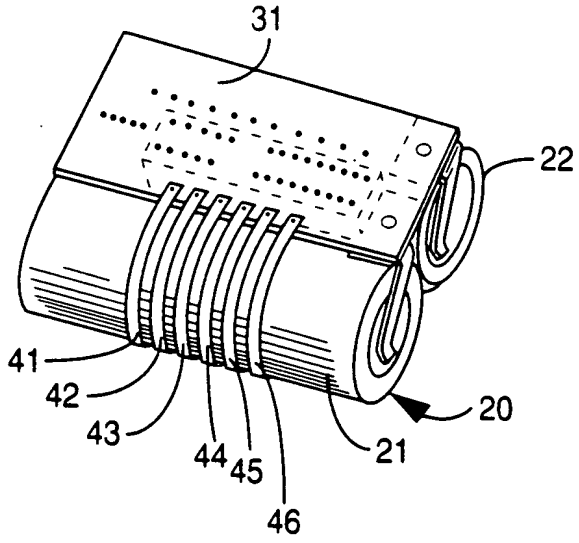


FIG. 3

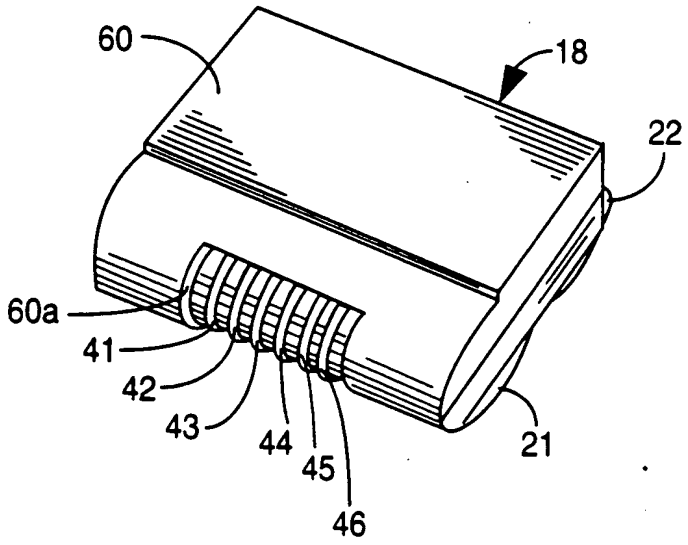


FIG. 4

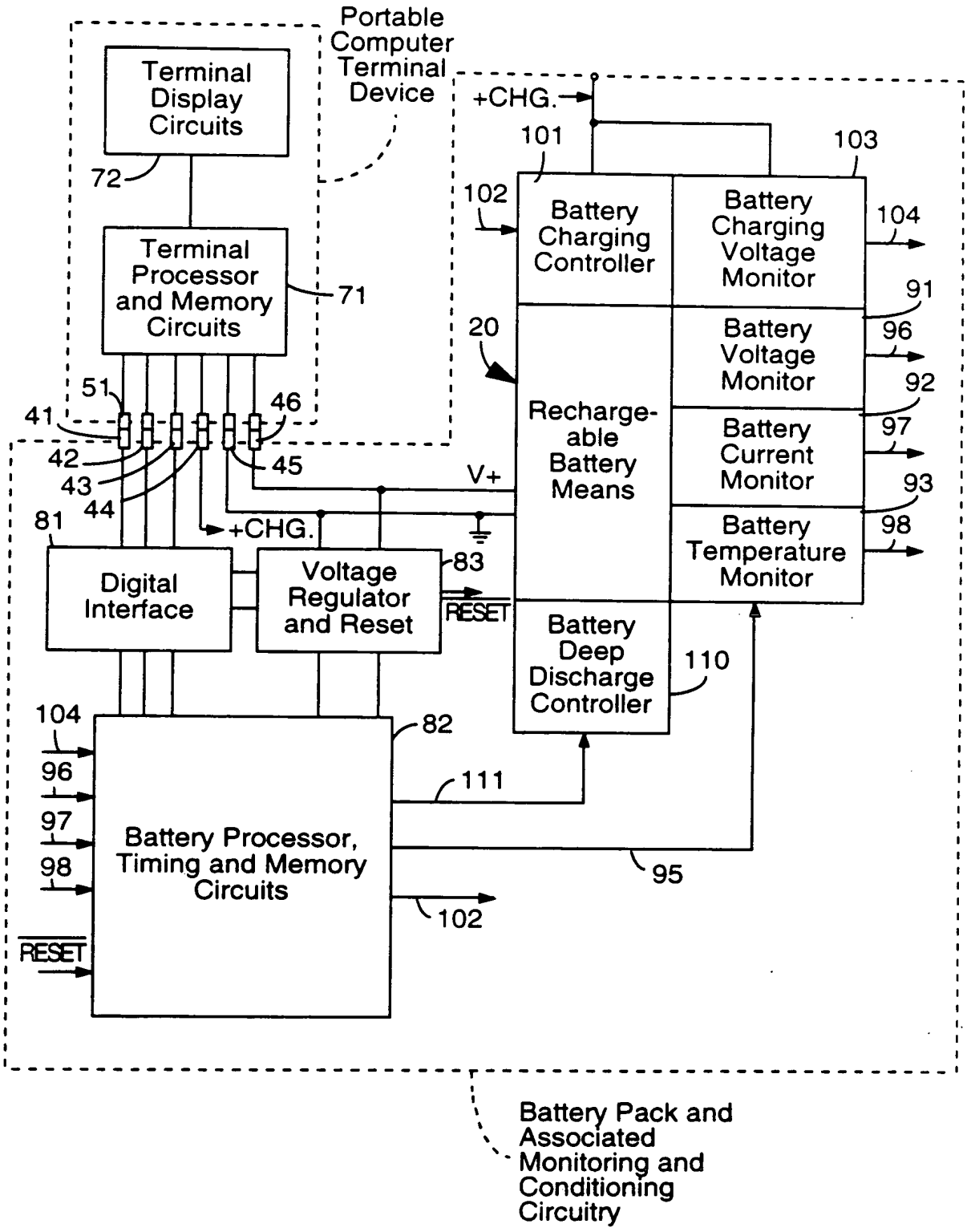

Portable Computer Terminal Device
Terminal Display Circuits
72
Terminal Processor and Memory Circuits
71
51
41
46
42
43
44
45
81
+CHG.
V+
Digital Interface
Voltage Regulator and Reset
83
RESET
+CHG.
101
103
102
Battery Charging Controller
Battery Charging Voltage Monitor
104
91
20
Battery Voltage Monitor
96
92
Recharge-able Battery Means
Battery Current Monitor
97
93
Battery Temperature Monitor
98
Battery Deep Discharge Controller
110
104
96
97
98
RESET
Battery Processor, Timing and Memory Circuits
82
111
95
102
Battery Pack and Associated Monitoring and Conditioning Circuitry

FIG. 5

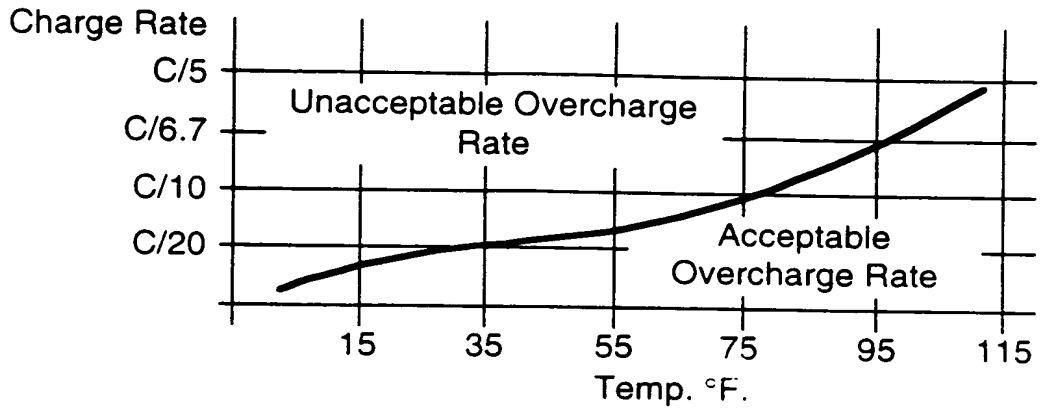


FIG. 6

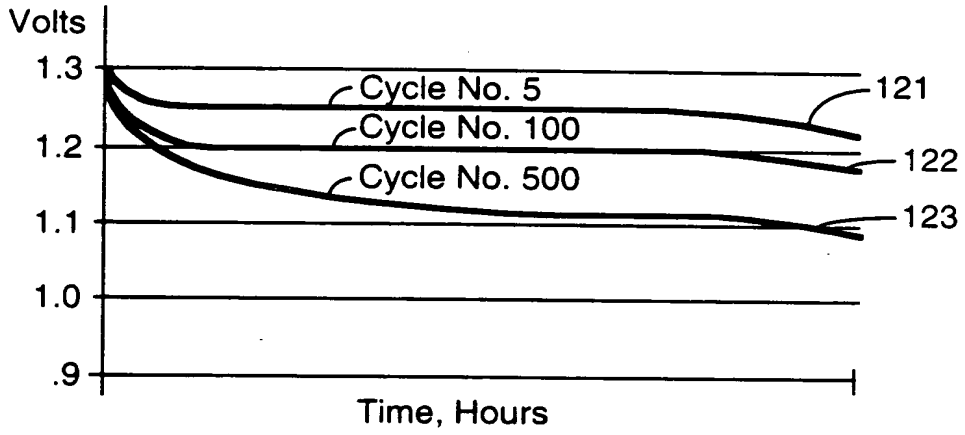


FIG. 7

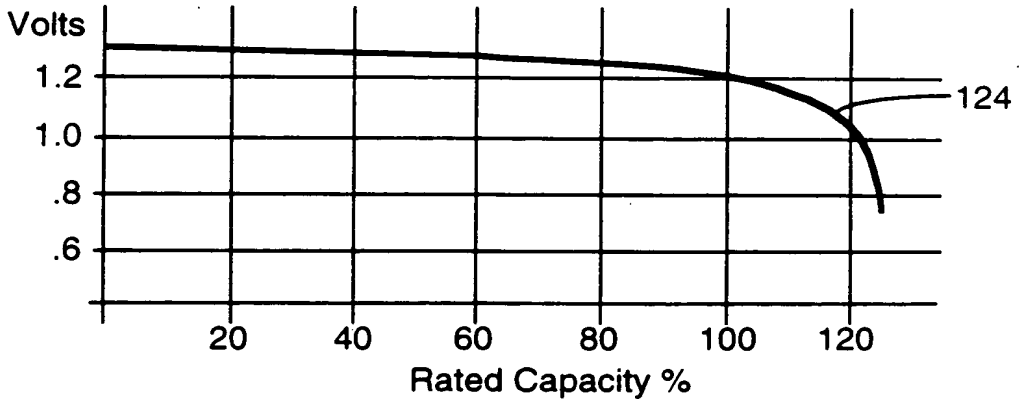


FIG. 8

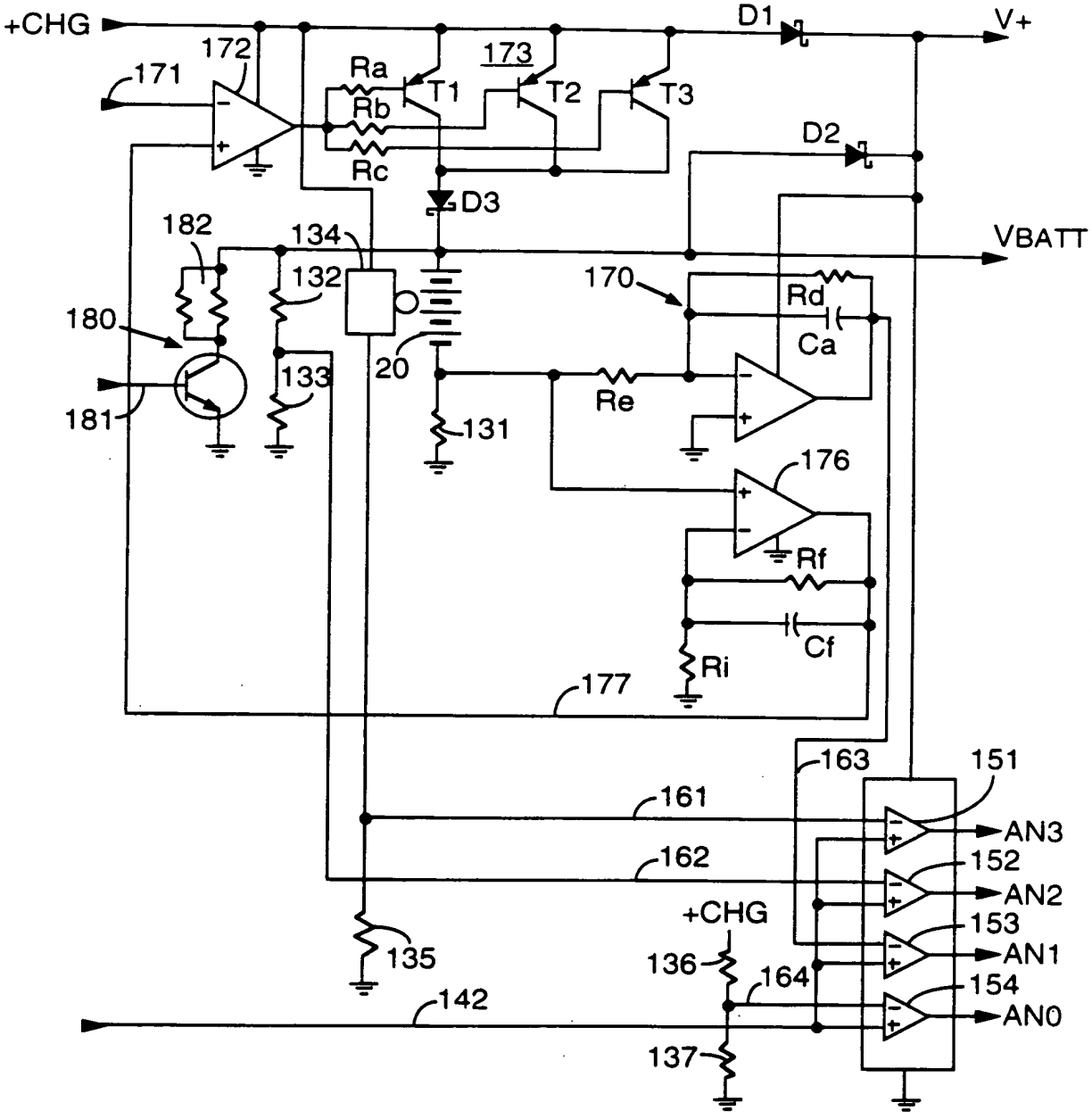

+CHG
D1
V+
172
171
Ra
173
T1
T2
T3
Rb
Rc
D2
D3
182
134
VBATT
132
170
Rd
180
Ca
133
20
Re
181
131
176
Rf
Cf
Ri
177
163
151
161
AN3
162
152
AN2
+CHG
153
135
136
AN1
164
154
142
AN0
137

FIG. 9A

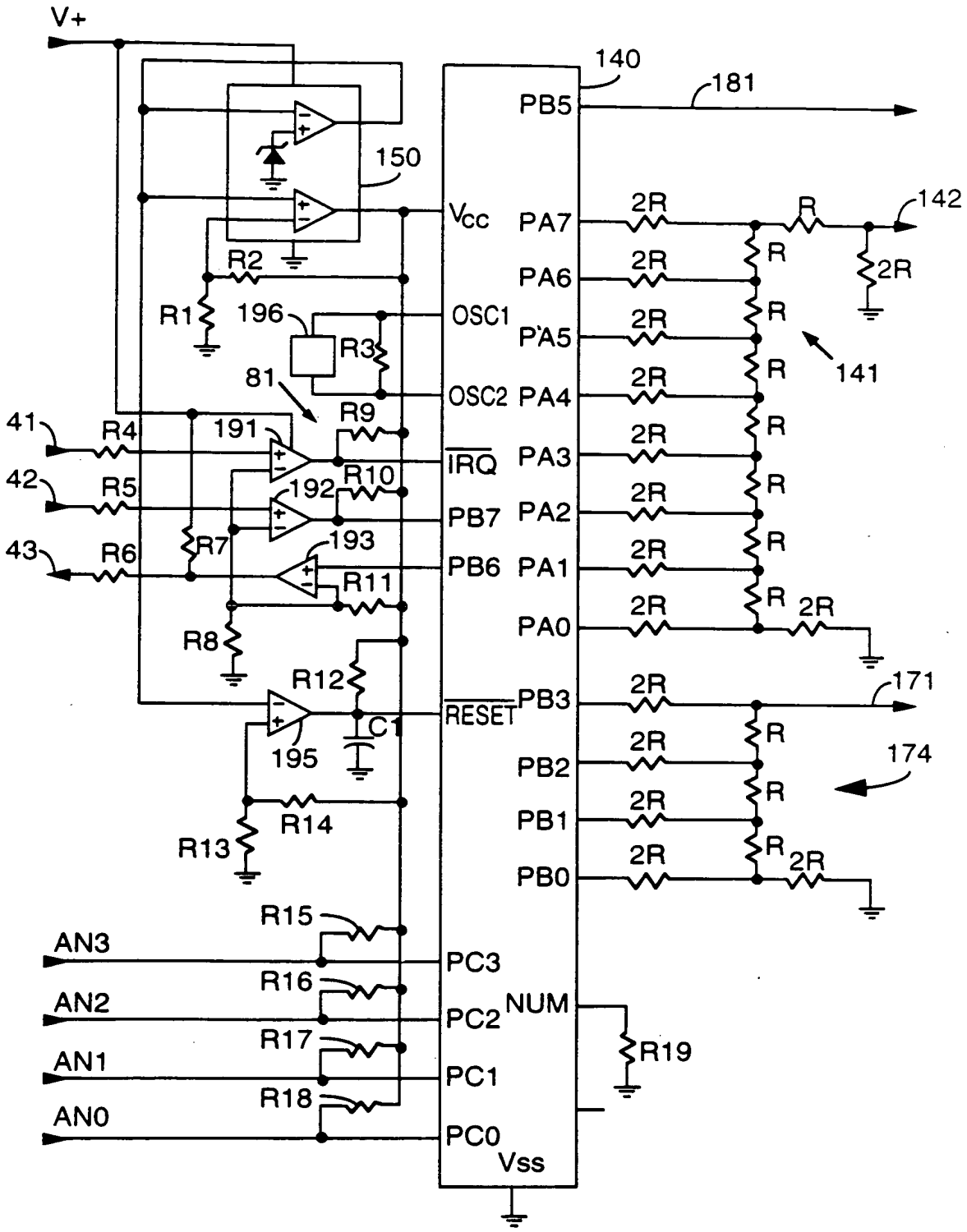

V+
140
181
PB5
150
Vcc
PA7
2R
R
142
R2
PA6
R1
196
OSC1
PA5
R3
141
81
OSC2
PA4
41
R4
191
R9
IRQ
PA3
42
R5
192
R10
PB7
PA2
43
R6
R7
193
PB6
PA1
R11
PA0
R8
R12
171
PB3
RESET
C1
195
174
PB2
R14
PB1
R13
PB0
R15
AN3
PC3
R16
AN2
PC2
NUM
R19
R17
AN1
PC1
R18
AN0
PC0
Vss

FIG. 9B

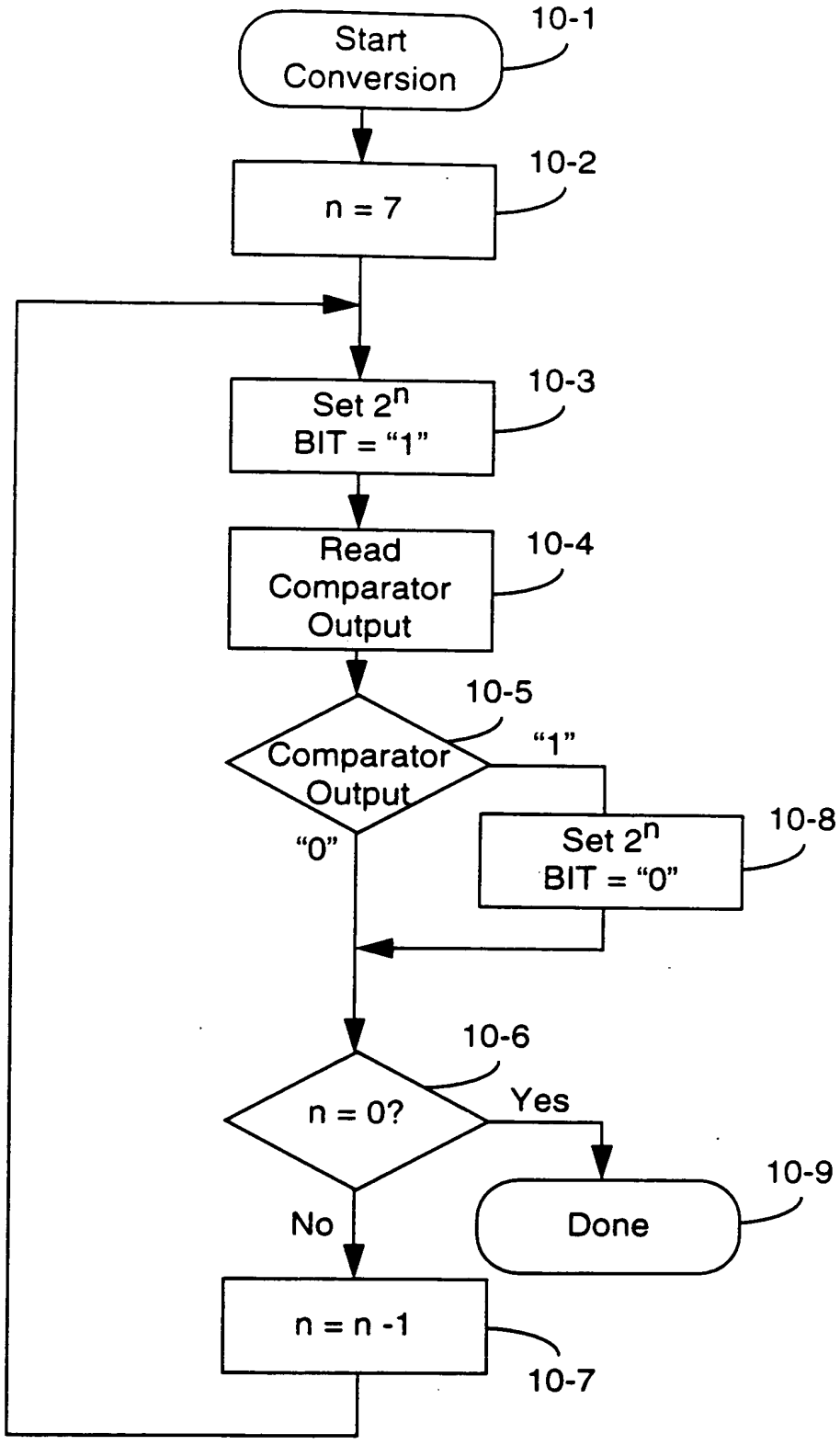

Start Conversion
10-1
n = 7
10-2
Set 2^n BIT = "1"
10-3
Read Comparator Output
10-4
Comparator Output
10-5
"1"
"0"
Set 2^n BIT = "0"
10-8
n = 0?
10-6
Yes
No
Done
10-9
n = n -1
10-7

FIG. 10

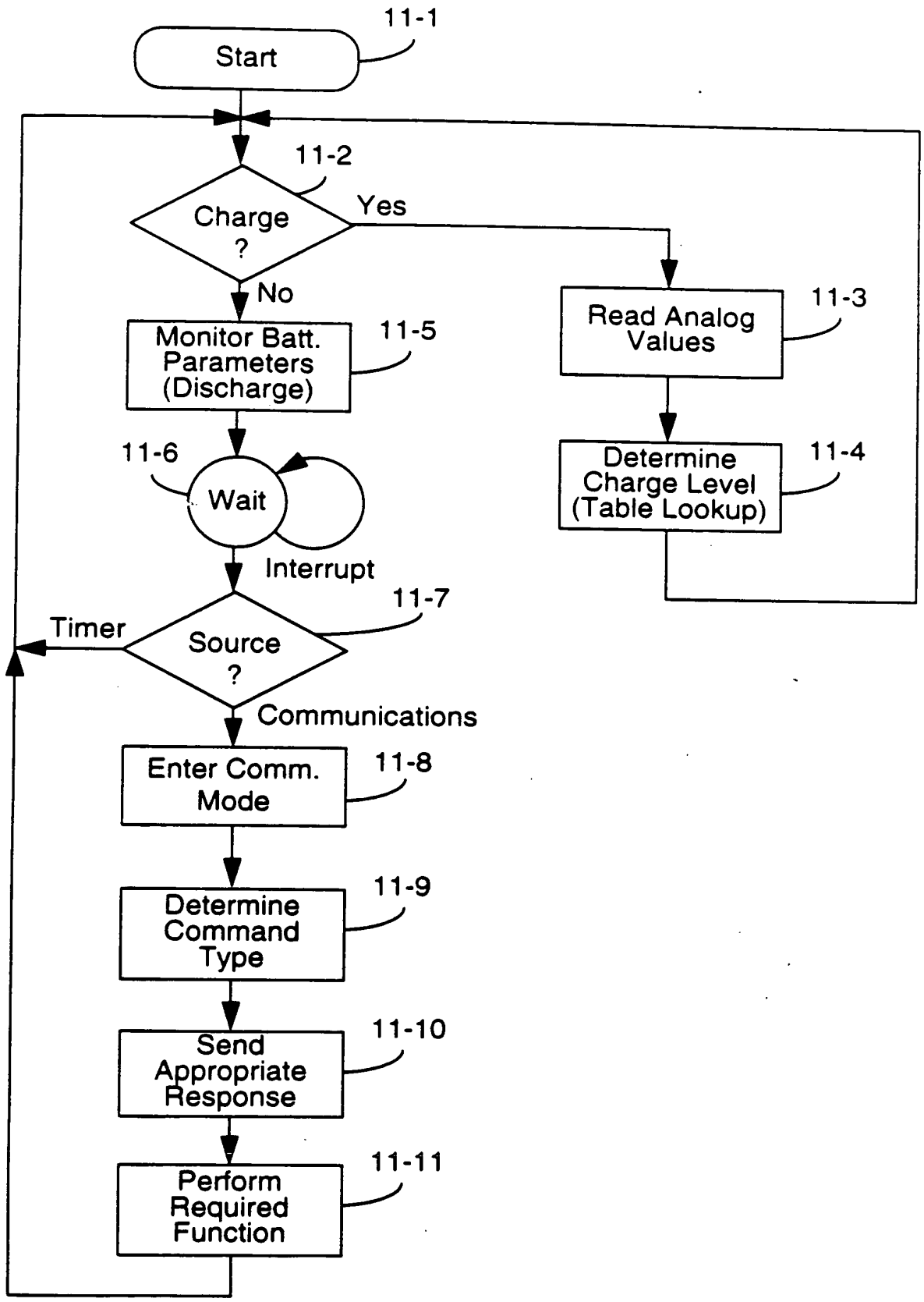

11-1
Start
11-2
Charge ?
Yes
No
11-3
Read Analog Values
11-4
Determine Charge Level (Table Lookup)
11-5
Monitor Batt. Parameters (Discharge)
11-6
Wait
Interrupt
11-7
Source ?
Timer
Communications
11-8
Enter Comm. Mode
11-9
Determine Command Type
11-10
Send Appropriate Response
11-11
Perform Required Function

FIG. 11

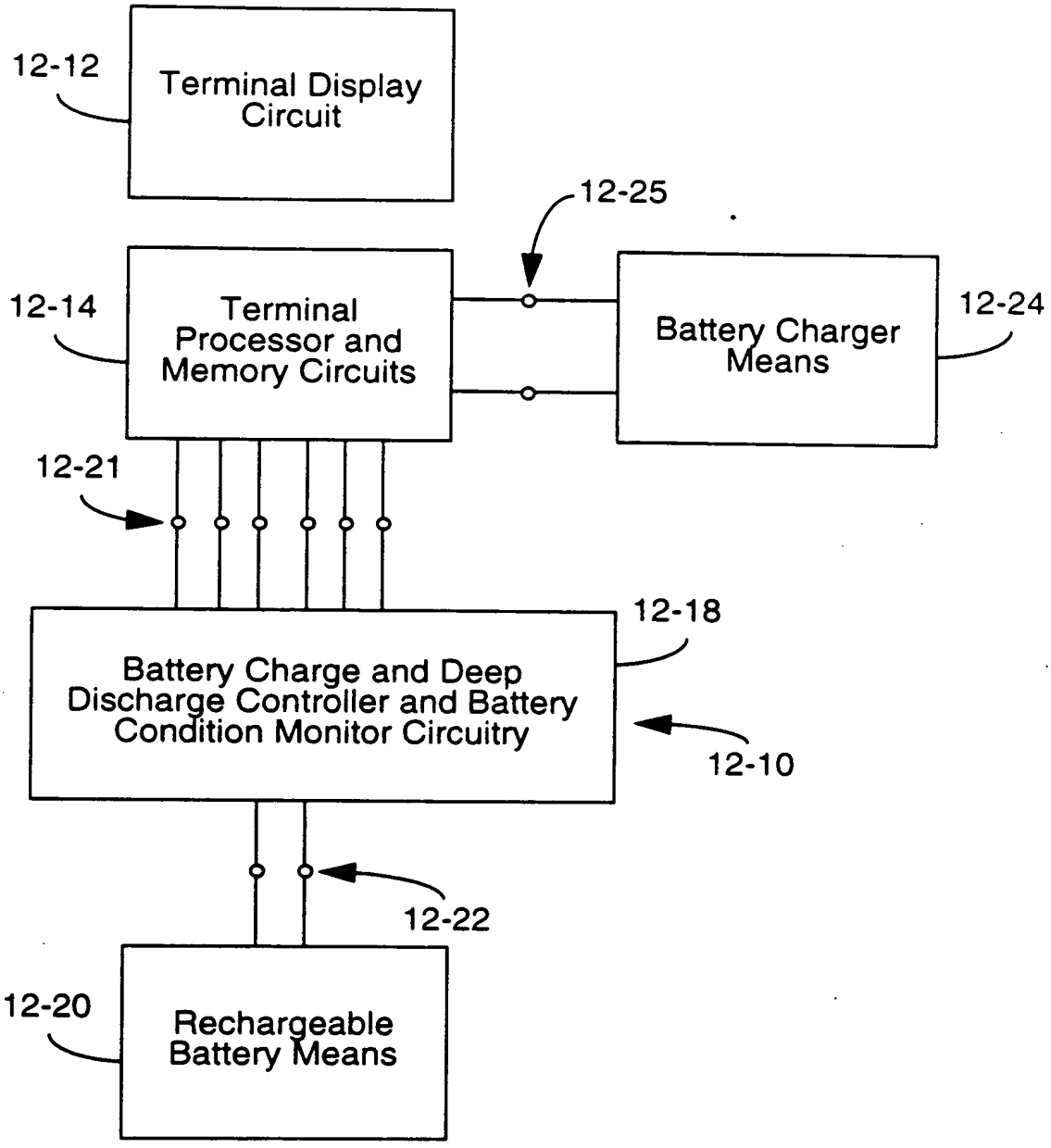

12-12
Terminal Display Circuit
12-25
12-14
Terminal Processor and Memory Circuits
Battery Charger Means
12-24
12-21
12-18
Battery Charge and Deep Discharge Controller and Battery Condition Monitor Circuitry
12-10
12-22
12-20
Rechargeable Battery Means

FIG. 12

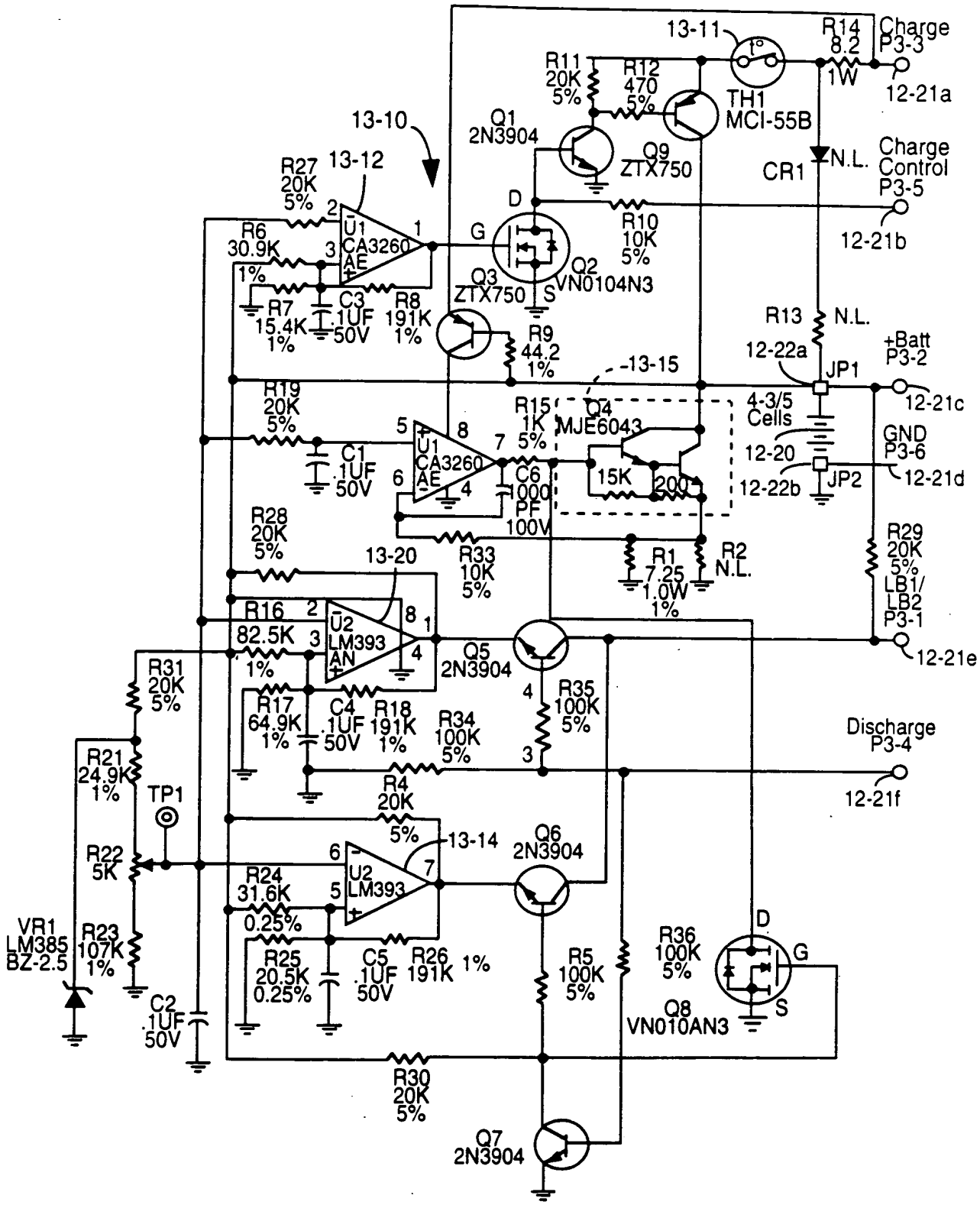

13-11
R14
8.2
1W
Charge
P3-3
12-21a
R11
20K
5%
R12
470
5%
TH1
MCI-55B
13-10
Q1
2N3904
Q9
ZTX750
CR1
N.L.
Charge
Control
P3-5
12-21b
R27
20K
5%
13-12
D
R10
10K
5%
R6
30.9K
1%
U1
CA3260
AE
G
Q2
VN0104N3
Q3
ZTX750
S
R7
15.4K
1%
C3
.1UF
50V
R8
191K
1%
R9
44.2
1%
R13
N.L.
12-22a
JP1
+Batt
P3-2
13-15
R19
20K
5%
R15
1K
5%
Q4
MJE6043
4-3/5
Cells
12-21c
GND
P3-6
C1
.1UF
50V
U1
CA3260
AE
C6
1000
PF
100V
15K
200
12-20
12-22b
JP2
12-21d
R28
20K
5%
R33
10K
5%
R1
7.25
1.0W
1%
R2
N.L.
R29
20K
5%
LB1/
LB2
P3-1
13-20
R16
82.5K
1%
U2
LM393
AN
Q5
2N3904
12-21e
R31
20K
5%
R17
64.9K
1%
C4
.1UF
50V
R18
191K
1%
R34
100K
5%
R35
100K
5%
Discharge
P3-4
R21
24.9K
1%
TP1
R4
20K
5%
12-21f
13-14
Q6
2N3904
R22
5K
R24
31.6K
0.25%
U2
LM393
VR1
LM385
BZ-2.5
R23
107K
1%
R25
20.5K
0.25%
C5
.1UF
50V
R26
191K
1%
R5
100K
5%
R36
100K
5%
D
G
S
Q8
VN010AN3
C2
.1UF
50V
R30
20K
5%
Q7
2N3904

FIG. 13

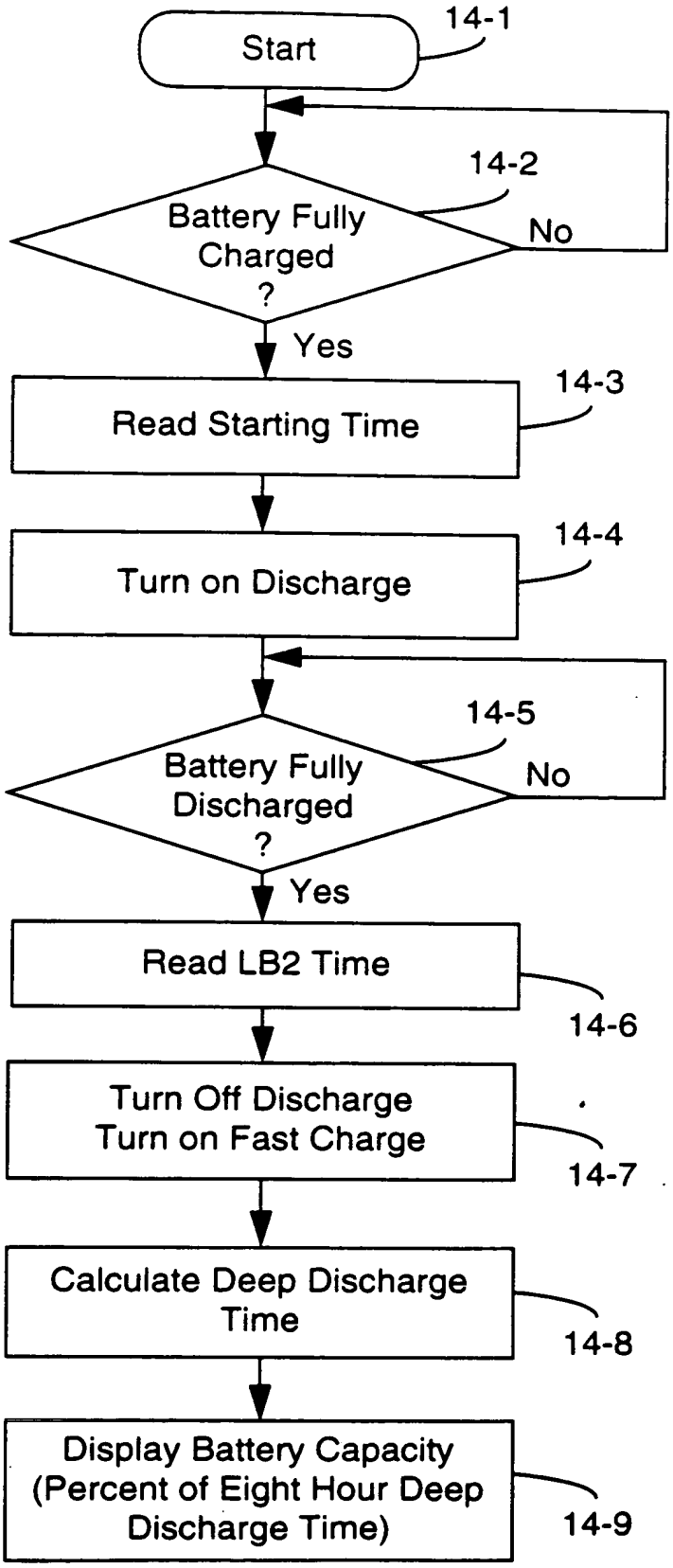

Start
14-1
Battery Fully Charged ?
14-2
No
Yes
Read Starting Time
14-3
Turn on Discharge
14-4
Battery Fully Discharged ?
14-5
No
Yes
Read LB2 Time
14-6
Turn Off Discharge
Turn on Fast Charge
14-7
Calculate Deep Discharge Time
14-8
Display Battery Capacity (Percent of Eight Hour Deep Discharge Time)
14-9

FIG. 14

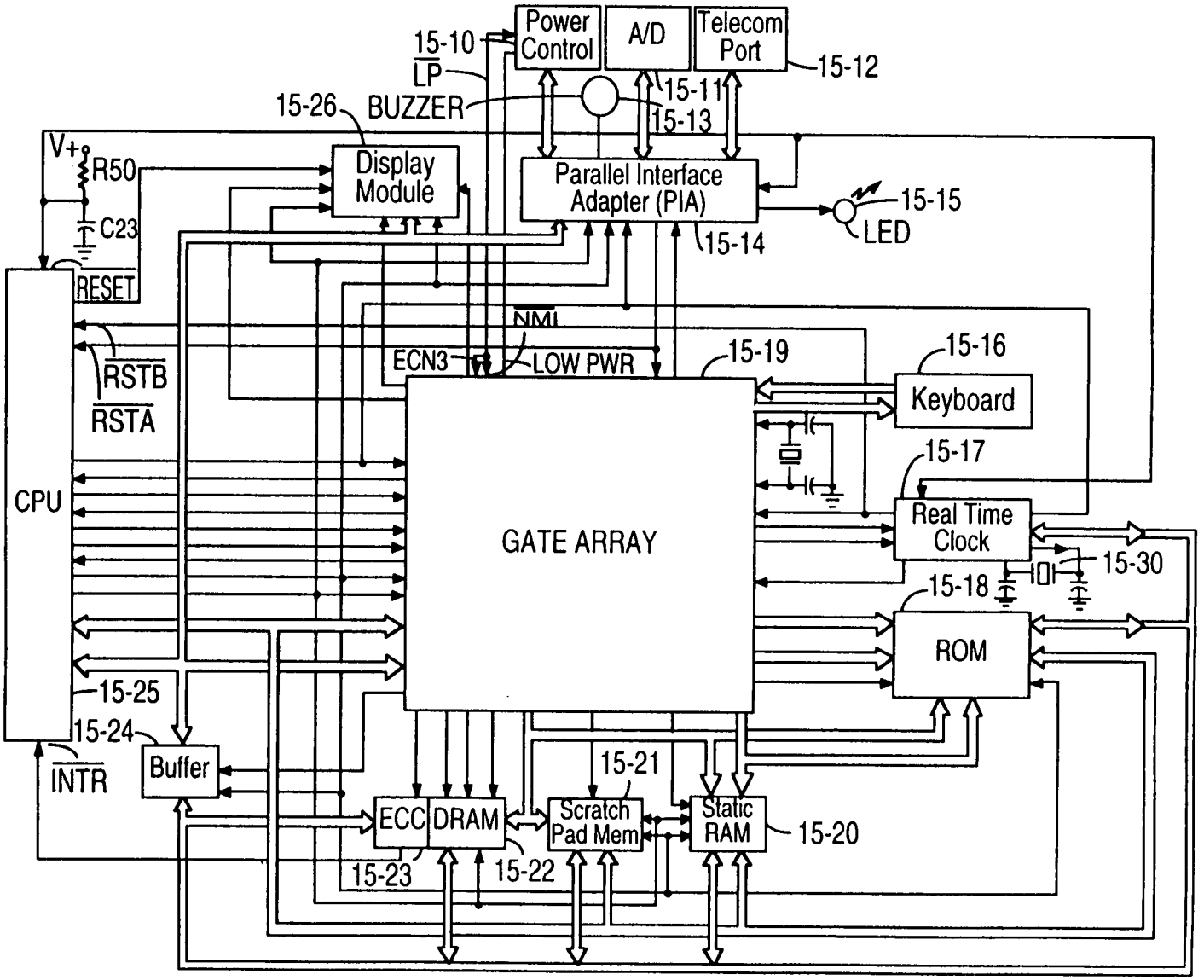


FIG. 15

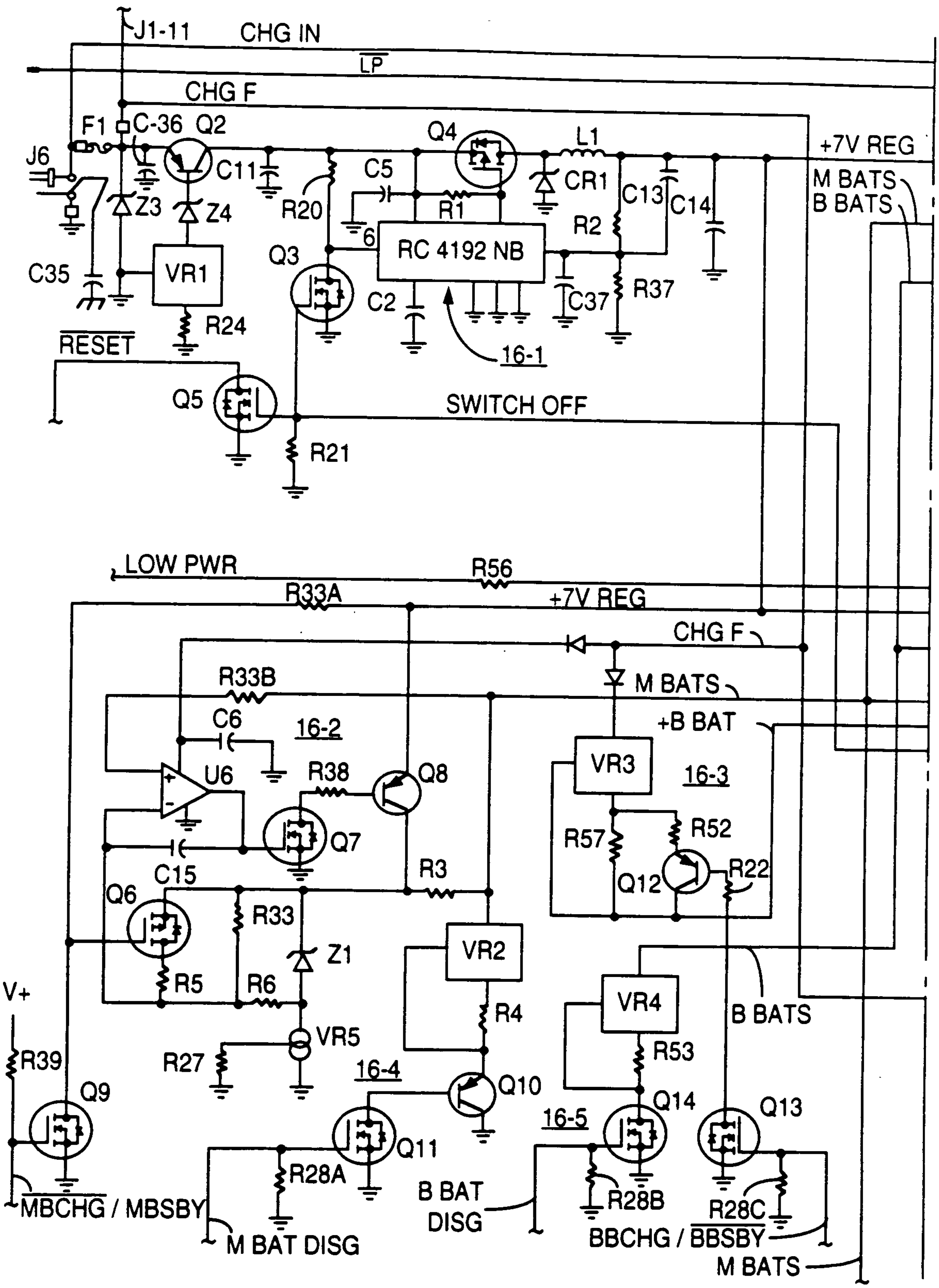

J1-11
CHG IN
LP
CHG F
F1
C-36
Q2
J6
C11
Q4
L1
+7V REG
C5
CR1
M BATS
B BATS
Z3
Z4
R20
R1
C13
C14
R2
6
RC 4192 NB
Q3
C35
VR1
C2
C37
R37
R24
16-1
RESET
Q5
SWITCH OFF
R21
LOW PWR
R56
R33A
+7V REG
CHG F
R33B
M BATS
+B BAT
C6
16-2
VR3
16-3
U6
R38
Q8
Q7
R57
R52
C15
R3
R22
Q6
Q12
R33
Z1
VR2
R5
R6
V+
R4
VR4
B BATS
VR5
R39
R27
16-4
R53
Q9
Q10
Q14
Q13
16-5
Q11
R28A
B BAT
DISG
R28B
R28C
MBCHG / MBSBY
M BAT DISG
BBCHG / BBSBY
M BATS

FIG. 16A

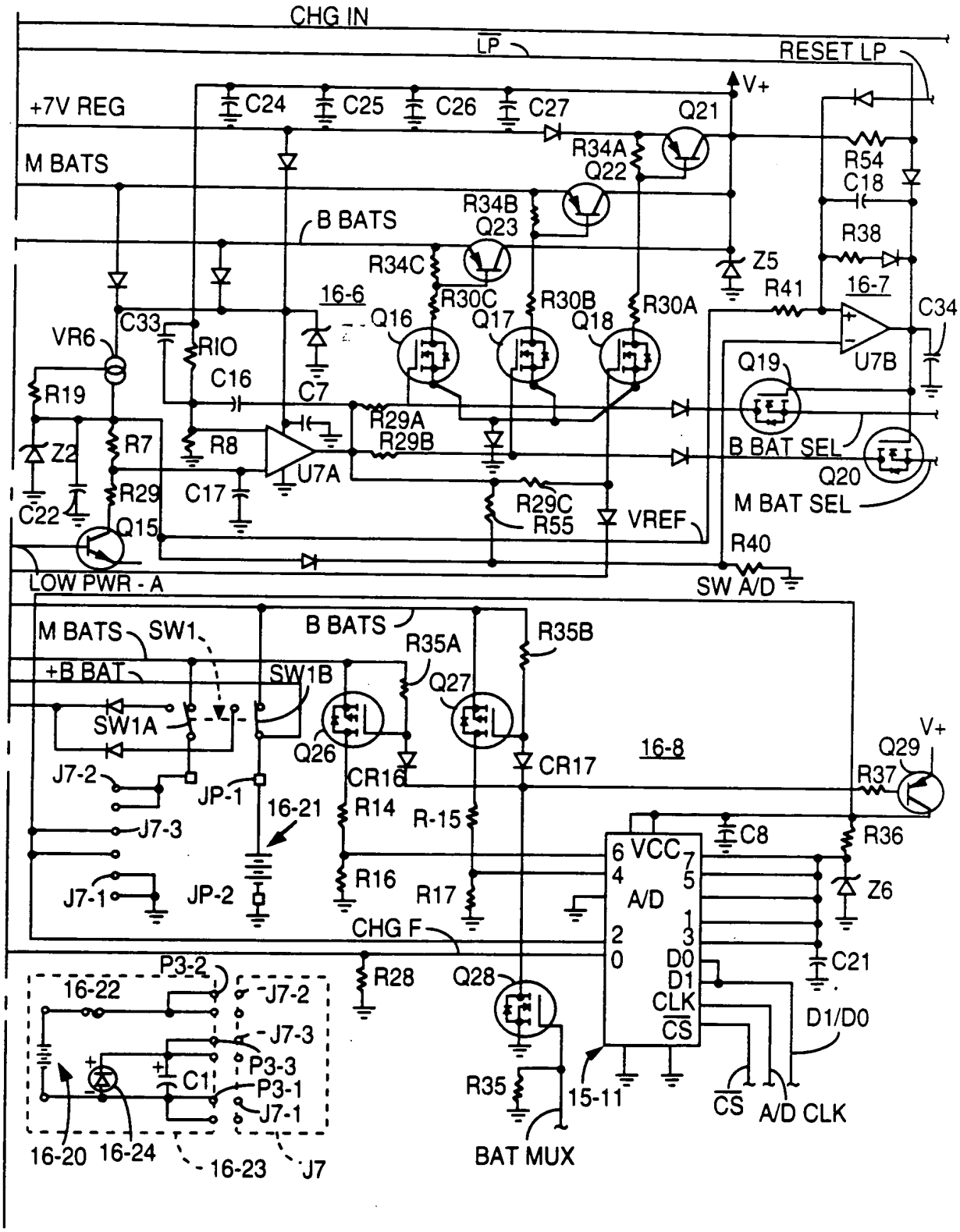

CHG IN
LP
RESET LP
V+
+7V REG
C24
C25
C26
C27
Q21
R34A
Q22
M BATS
B BATS
R34B
Q23
R34C
R30C
R30B
R30A
Z5
R41
16-7
C34
U7B
16-6
Q16
Q17
Q18
VR6
C33
RIO
C16
C7
R19
R29A
R29B
Q19
B BAT SEL
Z2
R7
R8
U7A
Q20
C22
R29
C17
R29C
R55
VREF
M BAT SEL
Q15
R40
LOW PWR - A
SW A/D
M BATS
SW1
B BATS
R35A
R35B
+B BAT
SW1B
Q27
SW1A
Q26
CR16
CR17
16-8
Q29
V+
J7-2
JP-1
16-21
R14
R-15
R37
J7-3
C8
R36
6 VCC 7
4 5
A/D
1
2 3
0 D0
D1
CLK
CS
J7-1
JP-2
R16
R17
Z6
CHG F
C21
P3-2
R28
Q28
16-22
J7-2
J7-3
P3-3
C1
P3-1
J7-1
D1/D0
R35
15-11
CS
A/D CLK
16-20
16-24
16-23
J7
BAT MUX

FIG. 16B

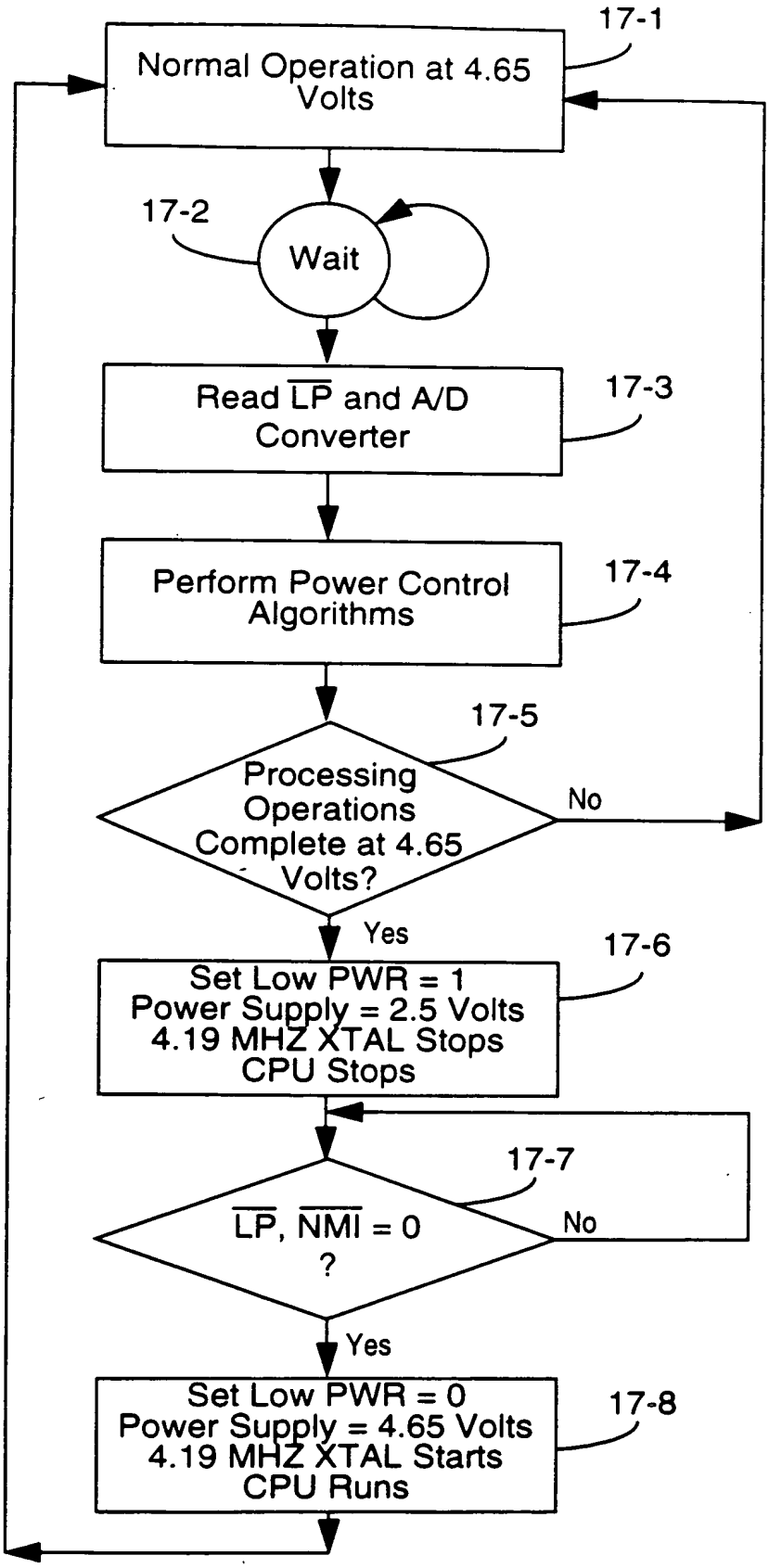

17-1
Normal Operation at 4.65 Volts
17-2
Wait
Read $\overline{LP}$ and A/D Converter
17-3
Perform Power Control Algorithms
17-4
17-5
Processing Operations Complete at 4.65 Volts?
No
Yes
17-6
Set Low PWR = 1
Power Supply = 2.5 Volts
4.19 MHZ XTAL Stops
CPU Stops
17-7
$\overline{LP}$, $\overline{NMI}$ = 0 ?
No
Yes
Set Low PWR = 0
Power Supply = 4.65 Volts
4.19 MHZ XTAL Starts
CPU Runs
17-8

FIG. 17

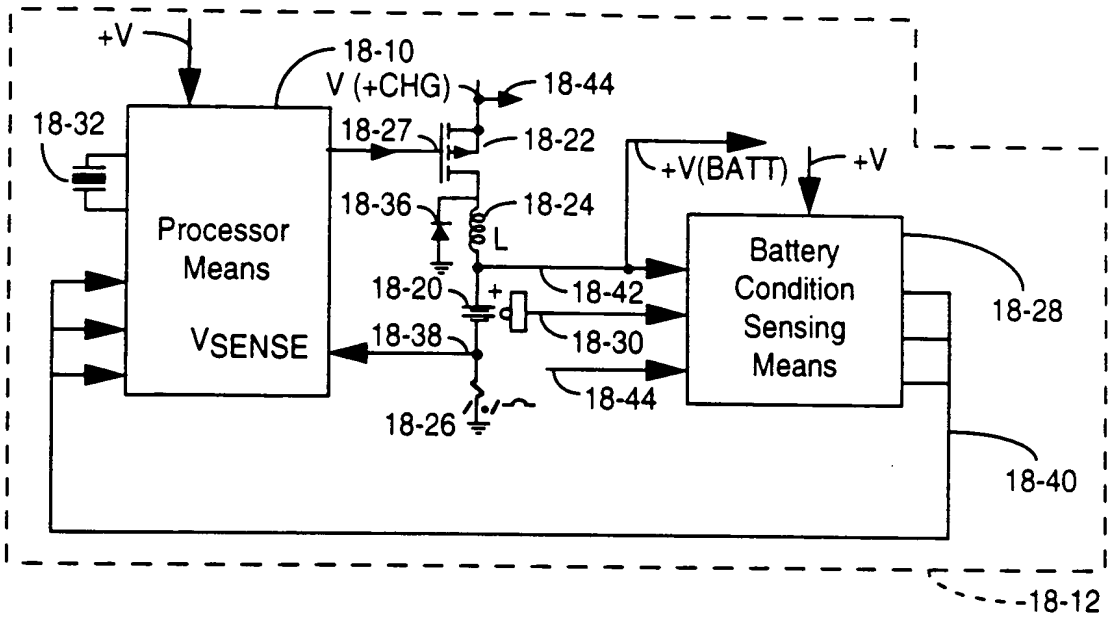

+V
18-10
V (+CHG)
18-44
18-32
18-27
18-22
+V(BATT)
+V
18-36
18-24
L
Processor
Means
VSENSE
18-20
18-42
Battery
Condition
Sensing
Means
18-28
18-38
18-30
18-44
18-26
18-40
18-12

FIG. 18

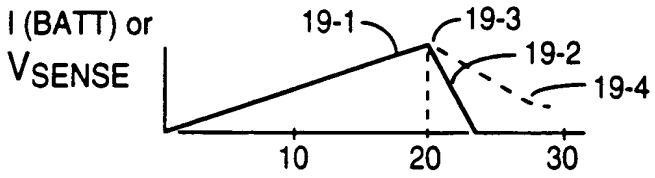

I (BATT) or
VSENSE
19-1
19-3
19-2
19-4
10
20
30

FIG. 19

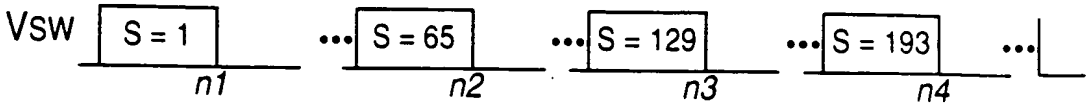


FIG. 20A

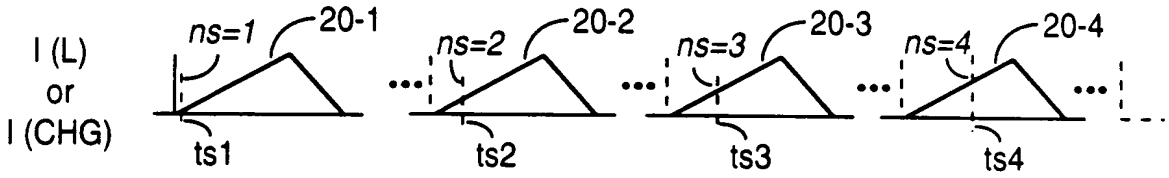


FIG. 20B

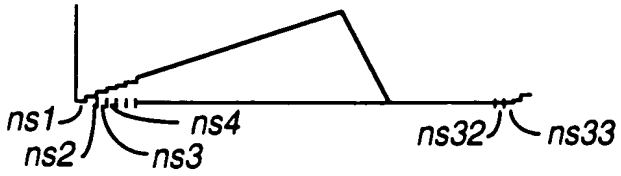


FIG. 21

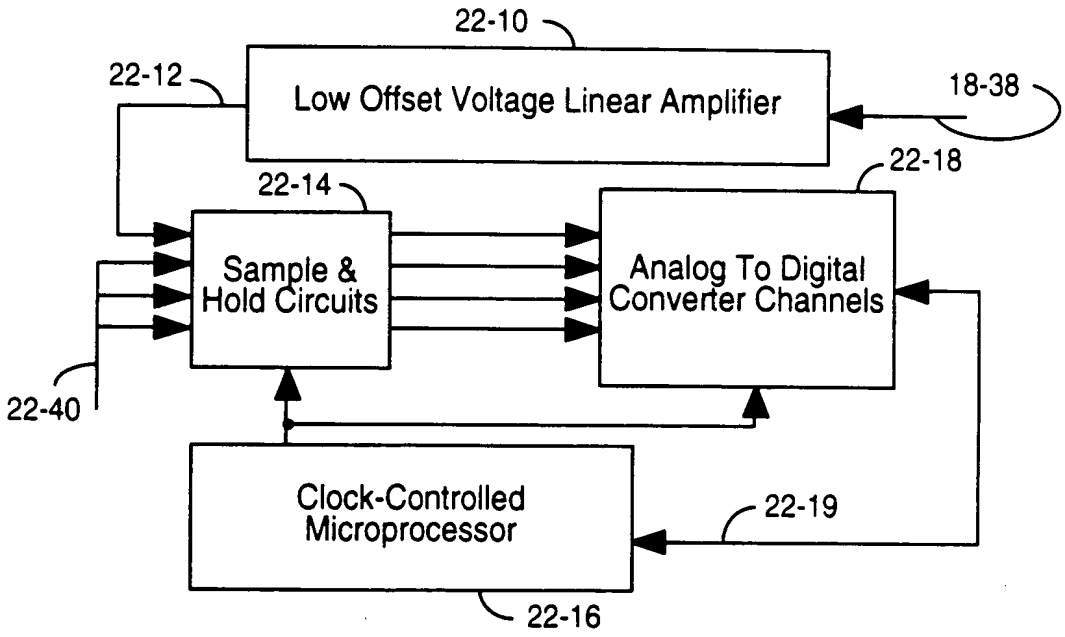

22-10
22-12
Low Offset Voltage Linear Amplifier
18-38
22-18
22-14
Sample &
Hold Circuits
Analog To Digital
Converter Channels
22-40
Clock-Controlled
Microprocessor
22-19
22-16

FIG. 22

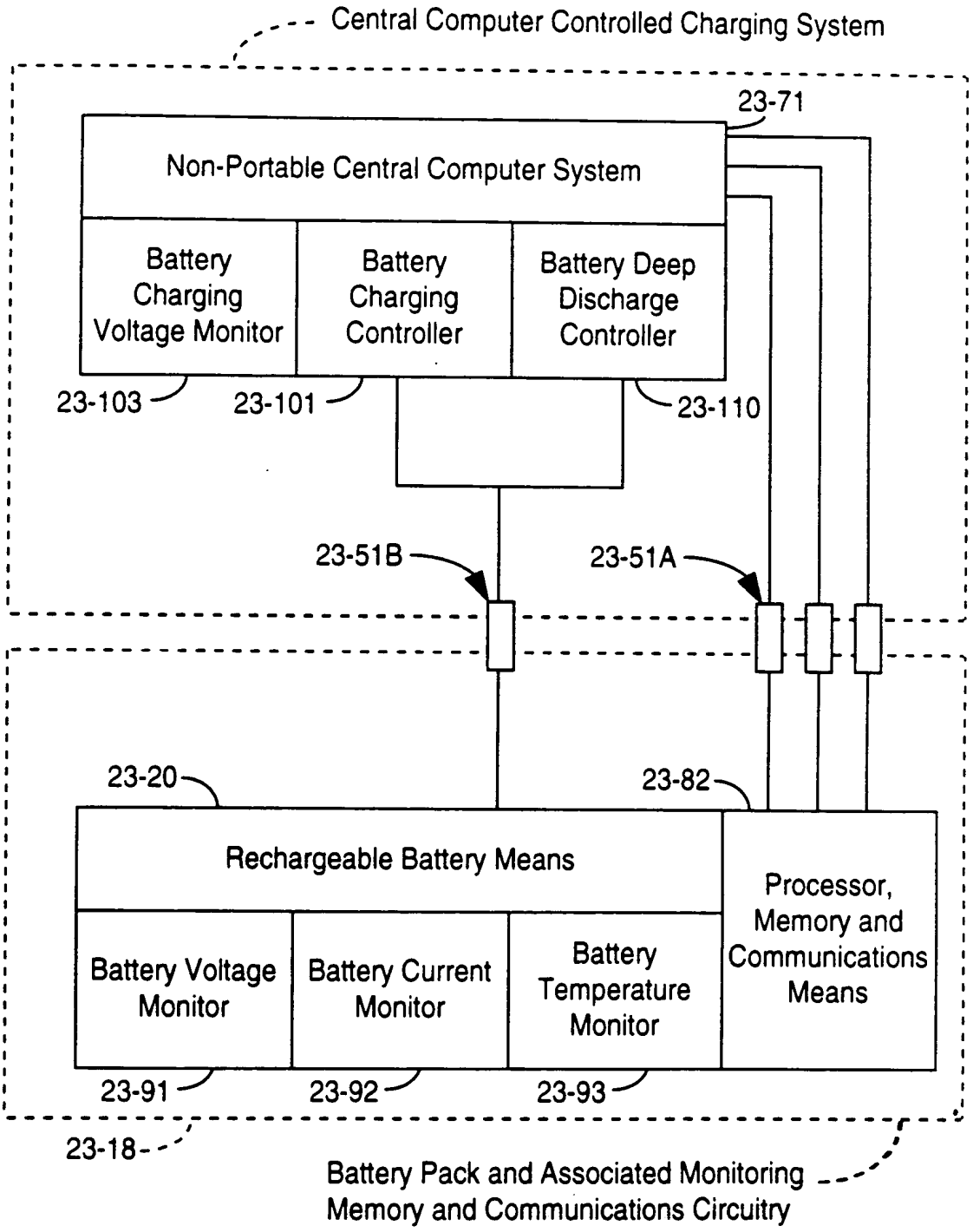

Central Computer Controlled Charging System
23-71
Non-Portable Central Computer System
Battery Charging Voltage Monitor
Battery Charging Controller
Battery Deep Discharge Controller
23-103
23-101
23-110
23-51B
23-51A
23-20
23-82
Rechargeable Battery Means
Processor, Memory and Communications Means
Battery Voltage Monitor
Battery Current Monitor
Battery Temperature Monitor
23-91
23-92
23-93
23-18
Battery Pack and Associated Monitoring Memory and Communications Circuitry

FIG. 23

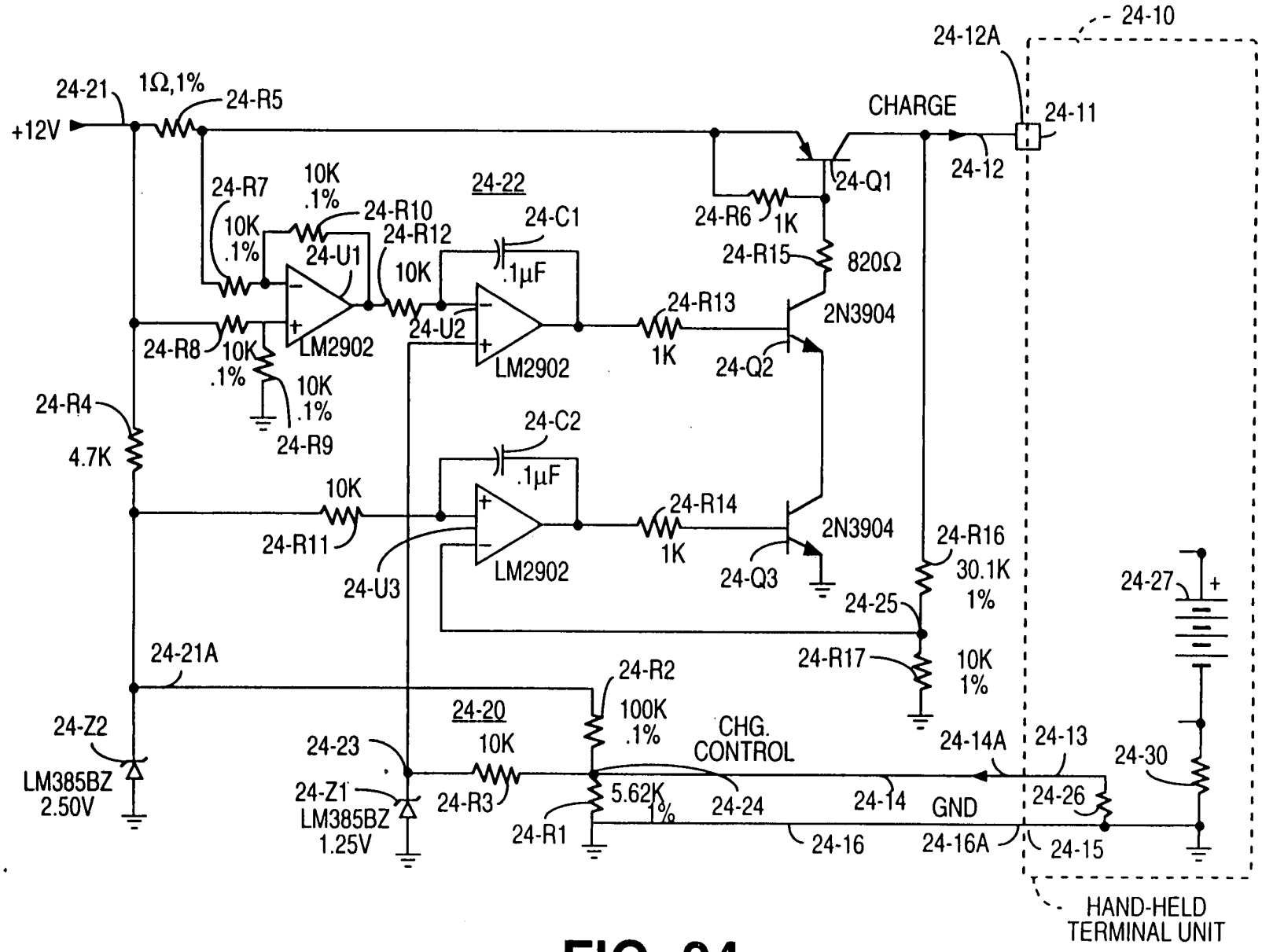


FIG. 24

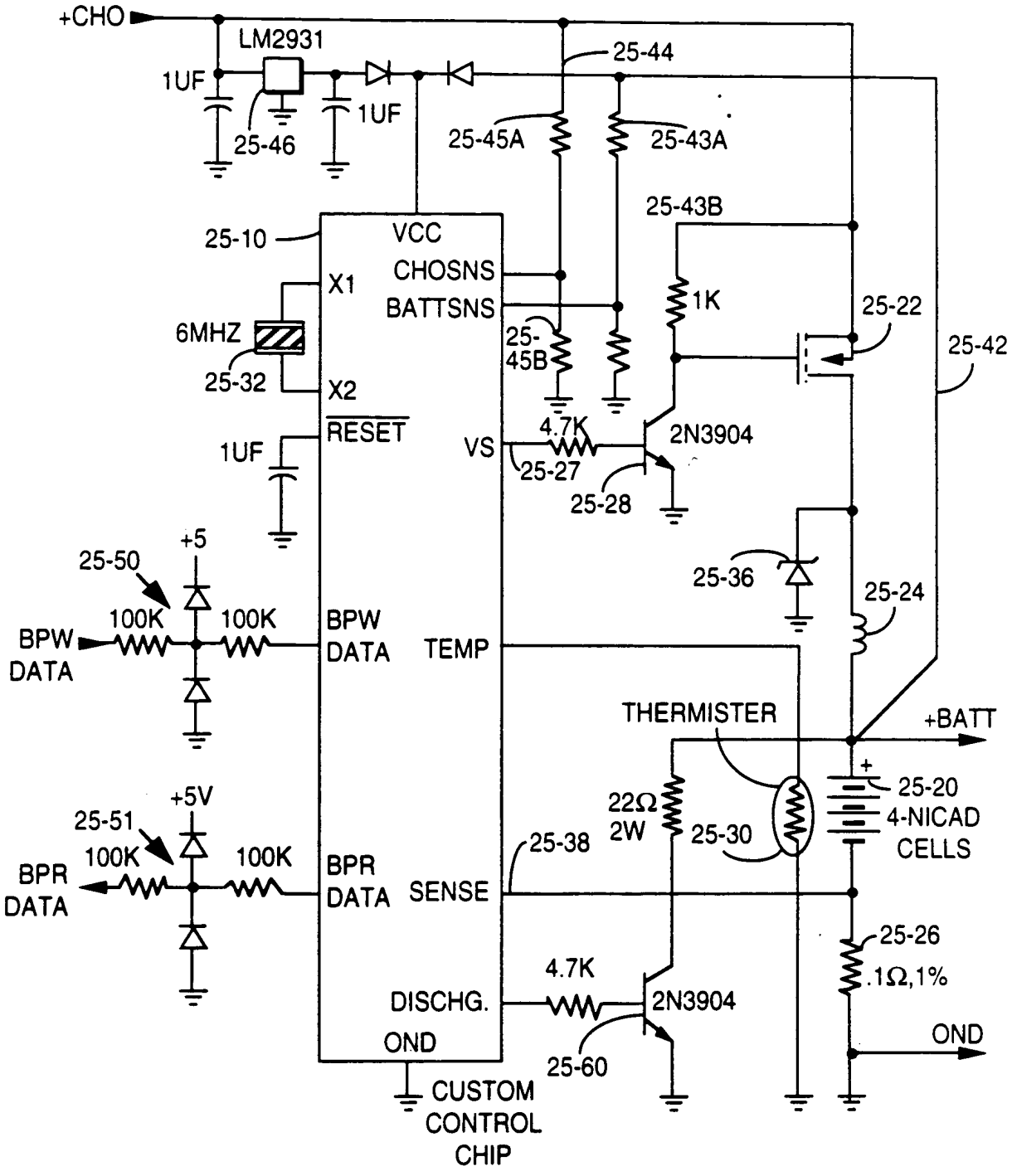

+CHO
LM2931
1UF
25-46
1UF
25-44
25-45A
25-43A
25-43B
25-10
VCC
CHOSNS
BATTSNS
X1
X2
6MHZ
25-32
25-
45B
1K
25-22
25-42
RESET
1UF
VS
4.7K
2N3904
25-27
25-28
+5
25-50
100K
100K
BPW
DATA
BPW
DATA
TEMP
25-36
25-24
THERMISTER
+BATT
+5V
25-51
100K
100K
BPR
DATA
BPR
DATA
SENSE
22Ω
2W
25-30
25-38
25-20
4-NICAD
CELLS
25-26
.1Ω,1%
4.7K
2N3904
DISCHG.
OND
25-60
OND
CUSTOM
CONTROL
CHIP

FIG. 25

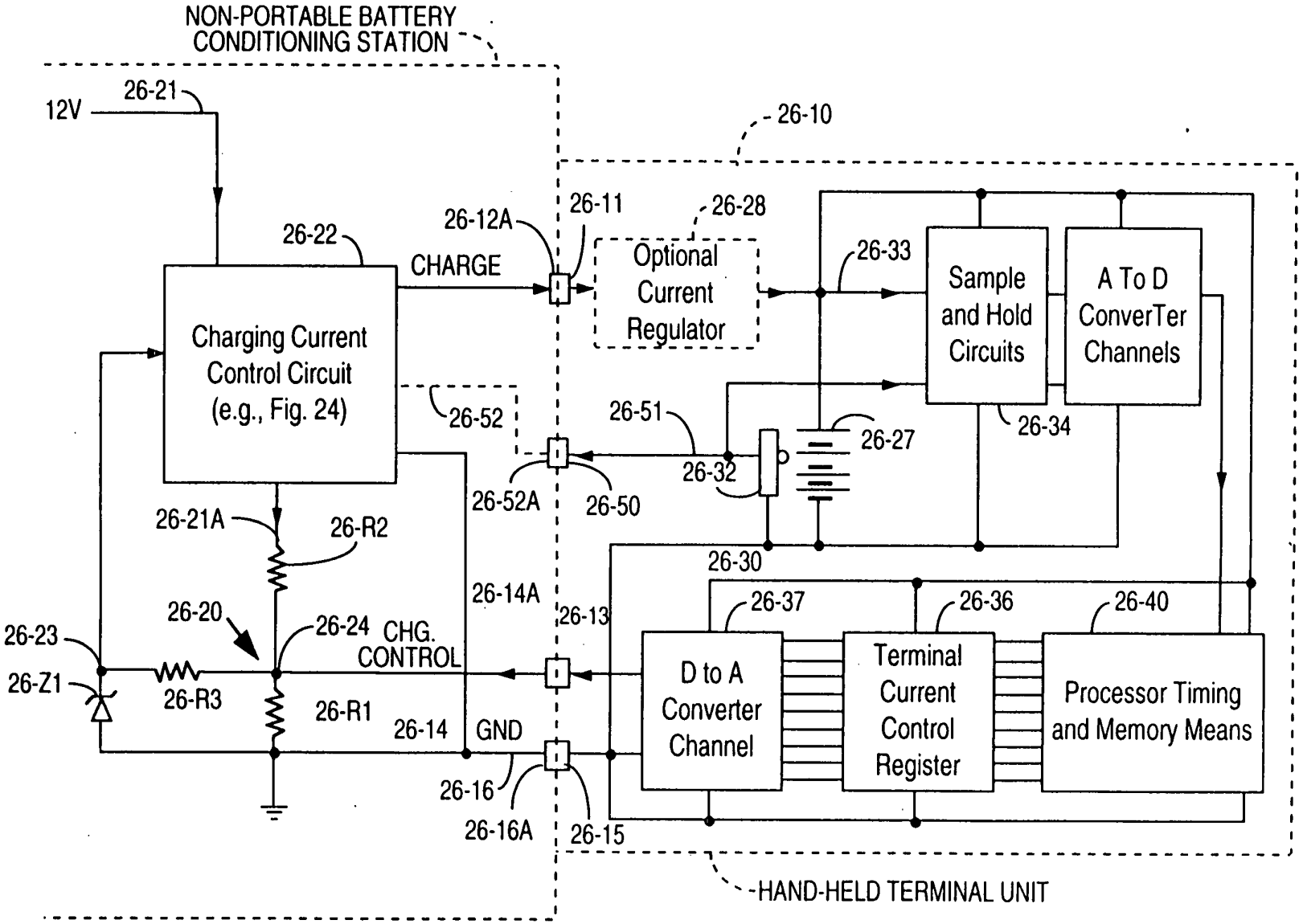

NON-PORTABLE BATTERY CONDITIONING STATION
12V
26-21
26-10
26-22
26-12A
26-11
26-28
CHARGE
Optional Current Regulator
26-33
Sample and Hold Circuits
A To D ConverTer Channels
Charging Current Control Circuit (e.g., Fig. 24)
26-52
26-51
26-27
26-34
26-32
26-52A
26-50
26-21A
26-R2
26-30
26-14A
26-13
26-37
26-36
26-40
26-20
26-24
CHG. CONTROL
26-23
26-Z1
26-R3
26-R1
26-14
GND
D to A Converter Channel
Terminal Current Control Register
Processor Timing and Memory Means
26-16
26-16A
26-15
HAND-HELD TERMINAL UNIT

FIG. 26

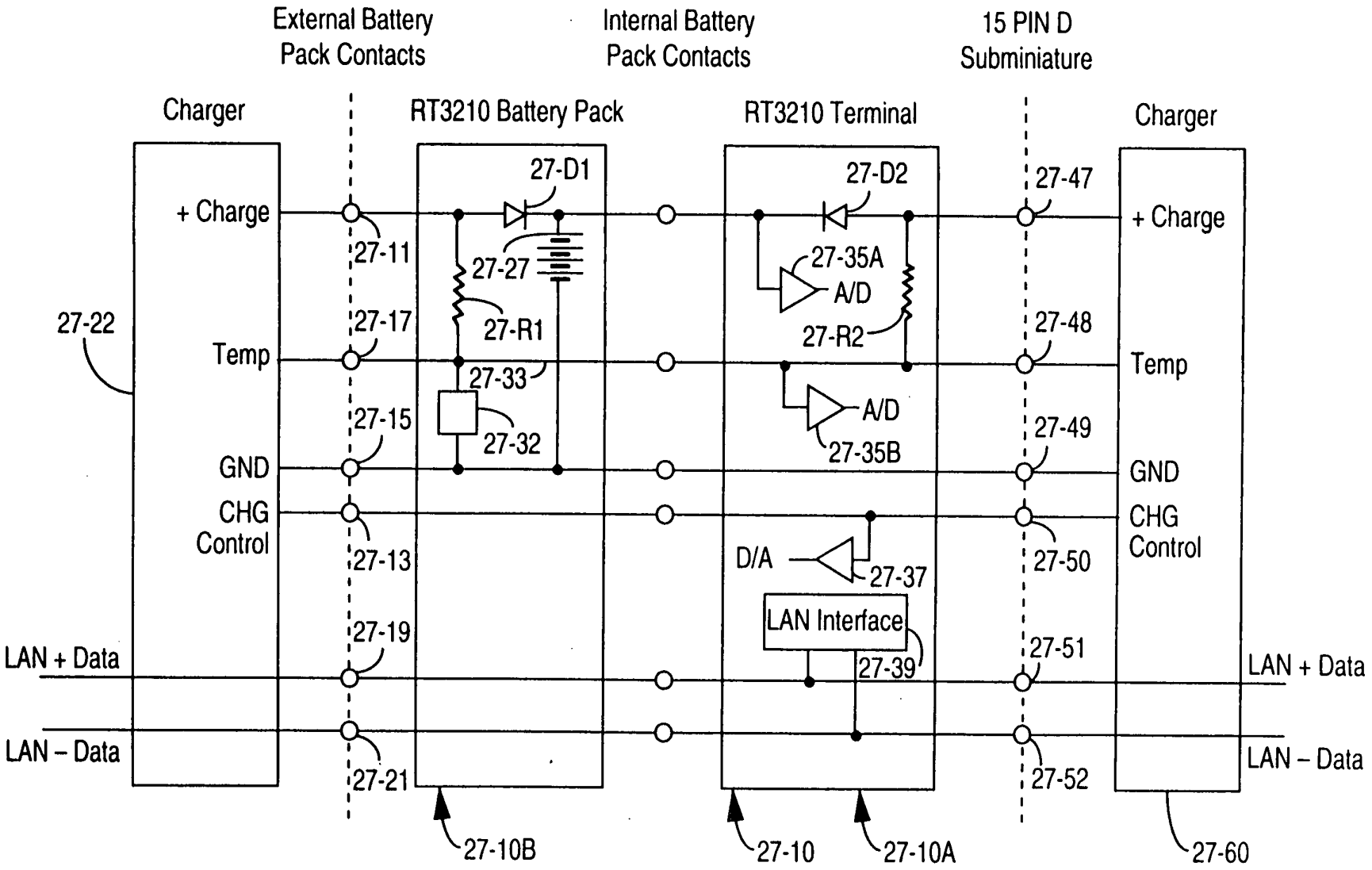

External Battery Pack Contacts
Internal Battery Pack Contacts
15 PIN D Subminiature
Charger
RT3210 Battery Pack
RT3210 Terminal
Charger
27-D1
27-D2
27-47
+ Charge
27-11
27-27
27-35A
A/D
27-R1
27-R2
27-22
27-17
27-48
Temp
27-33
A/D
27-15
27-49
27-32
27-35B
GND
CHG Control
27-13
D/A
27-37
27-50
LAN Interface
27-19
27-51
LAN + Data
27-39
LAN – Data
27-21
27-52
27-10B
27-10
27-10A
27-60

FIG. 27

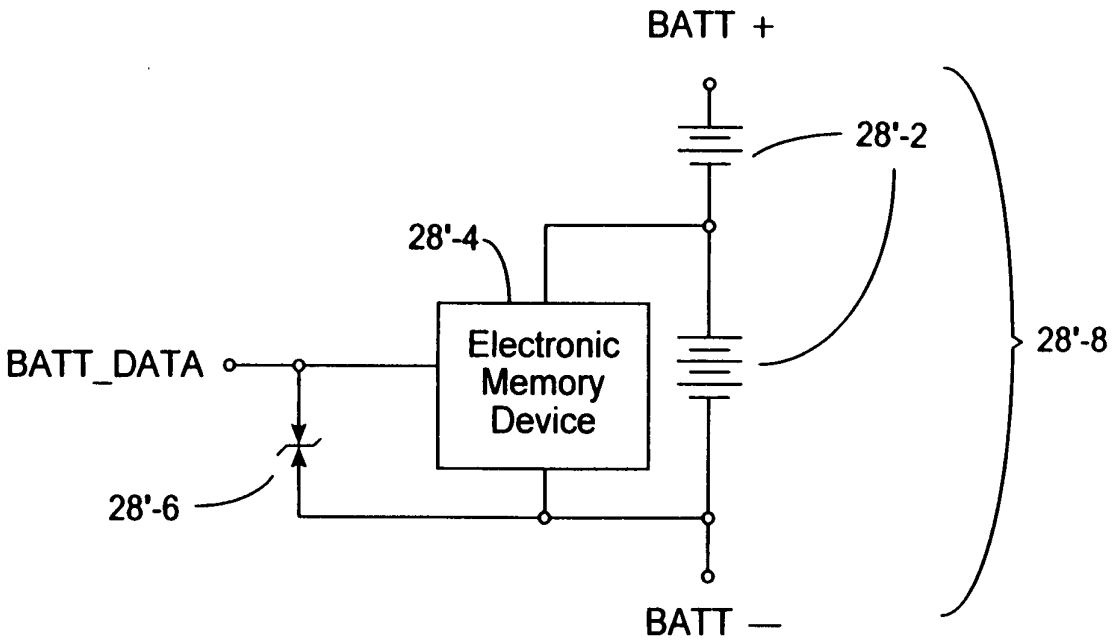

BATT +
28'-2
28'-4
Electronic
Memory
Device
BATT_DATA
28'-8
28'-6
BATT —

FIG. 28'

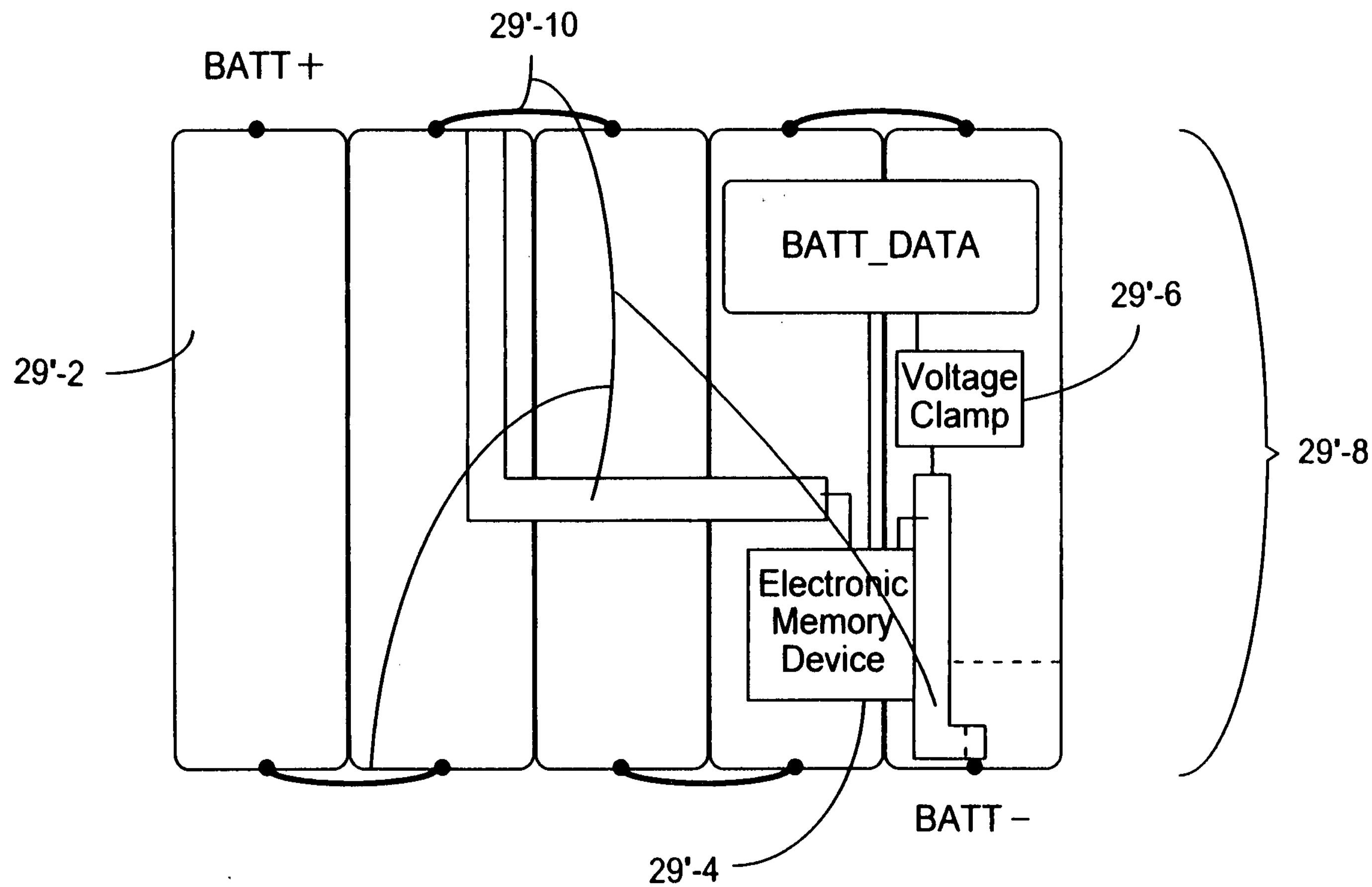

29'-10
BATT +
29'-2
BATT_DATA
29'-6
Voltage Clamp
29'-8
Electronic Memory Device
BATT −
29'-4

FIG. 29'

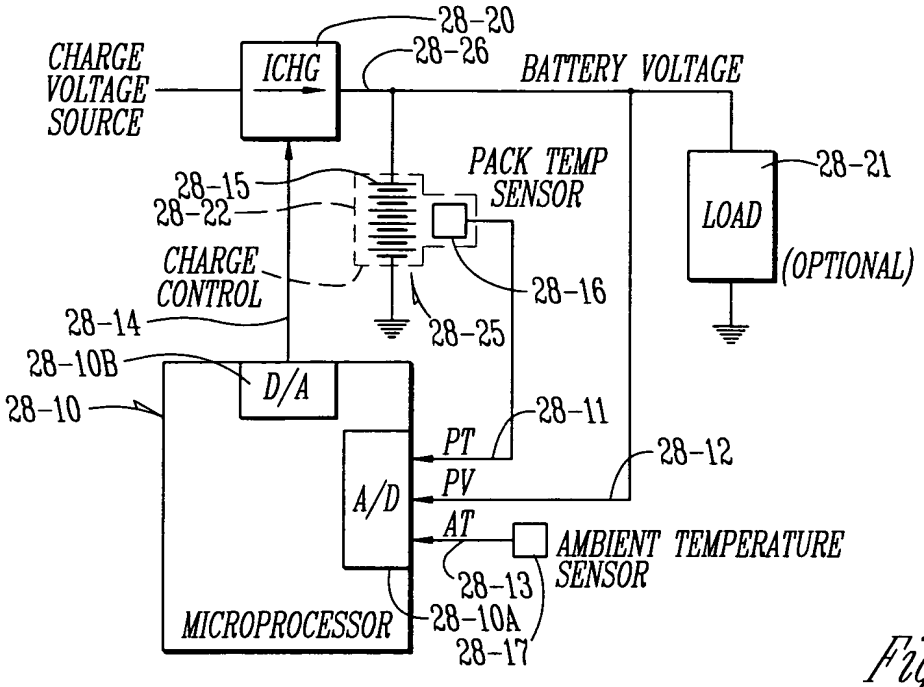

28-20
CHARGE VOLTAGE SOURCE
ICHG
28-26
BATTERY VOLTAGE
PACK TEMP SENSOR
28-15
28-22
LOAD
28-21
(OPTIONAL)
CHARGE CONTROL
28-16
28-14
28-25
28-10B
D/A
28-10
28-11
PT
28-12
PV
A/D
AT
AMBIENT TEMPERATURE SENSOR
28-13
MICROPROCESSOR
28-10A
28-17

Fig. 28

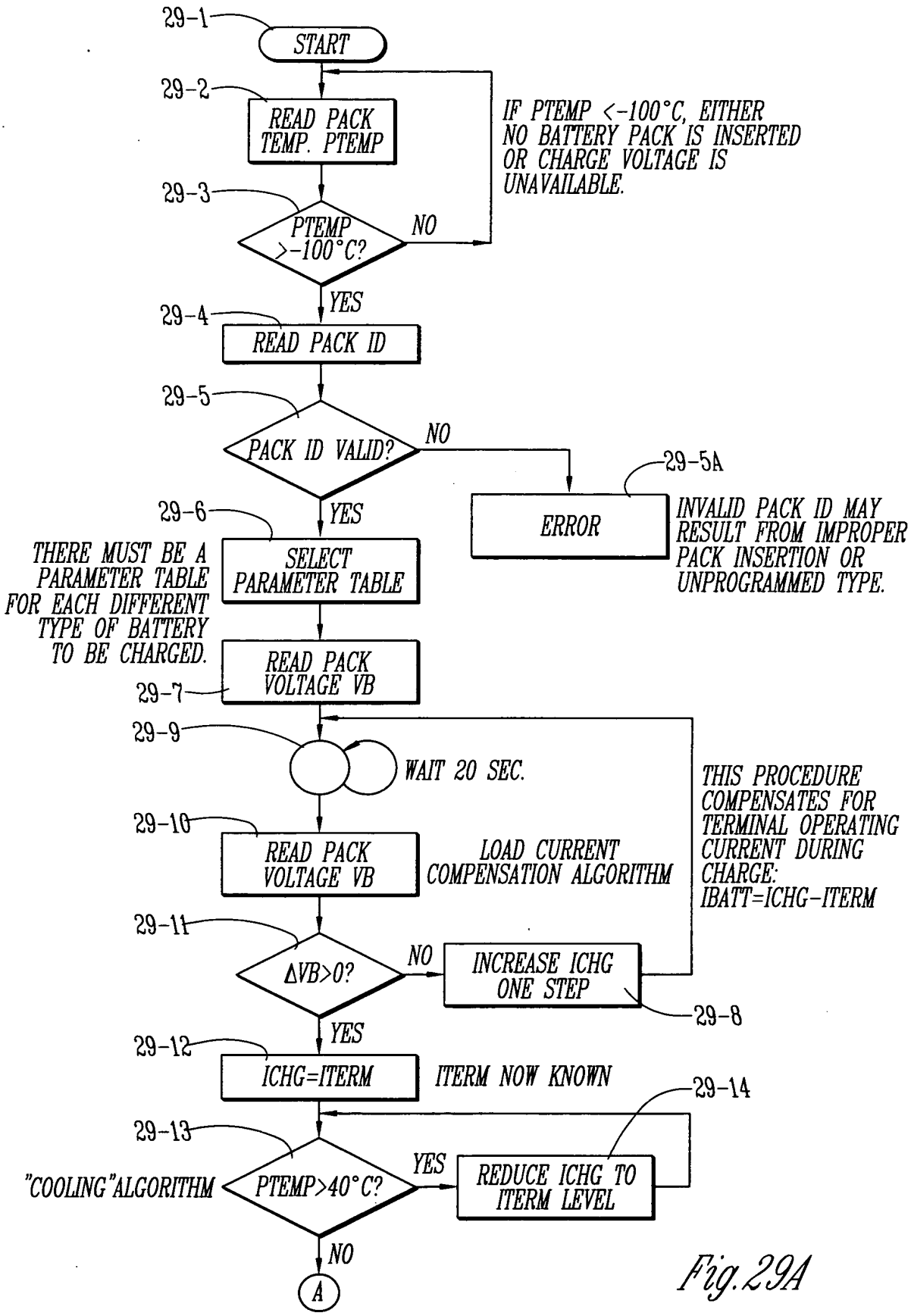

29-1
START
29-2
READ PACK TEMP. PTEMP
29-3
PTEMP >-100°C?
NO
YES
IF PTEMP <-100°C, EITHER NO BATTERY PACK IS INSERTED OR CHARGE VOLTAGE IS UNAVAILABLE.
29-4
READ PACK ID
29-5
PACK ID VALID?
NO
YES
29-5A
ERROR
INVALID PACK ID MAY RESULT FROM IMPROPER PACK INSERTION OR UNPROGRAMMED TYPE.
29-6
SELECT PARAMETER TABLE
THERE MUST BE A PARAMETER TABLE FOR EACH DIFFERENT TYPE OF BATTERY TO BE CHARGED.
READ PACK VOLTAGE VB
29-7
29-9
WAIT 20 SEC.
THIS PROCEDURE COMPENSATES FOR TERMINAL OPERATING CURRENT DURING CHARGE: IBATT=ICHG-ITERM
29-10
READ PACK VOLTAGE VB
LOAD CURRENT COMPENSATION ALGORITHM
29-11
ΔVB>0?
NO
INCREASE ICHG ONE STEP
29-8
YES
29-12
ICHG=ITERM
ITERM NOW KNOWN
29-14
29-13
"COOLING" ALGORITHM
PTEMP>40°C?
YES
REDUCE ICHG TO ITERM LEVEL
NO
A

Fig. 29A

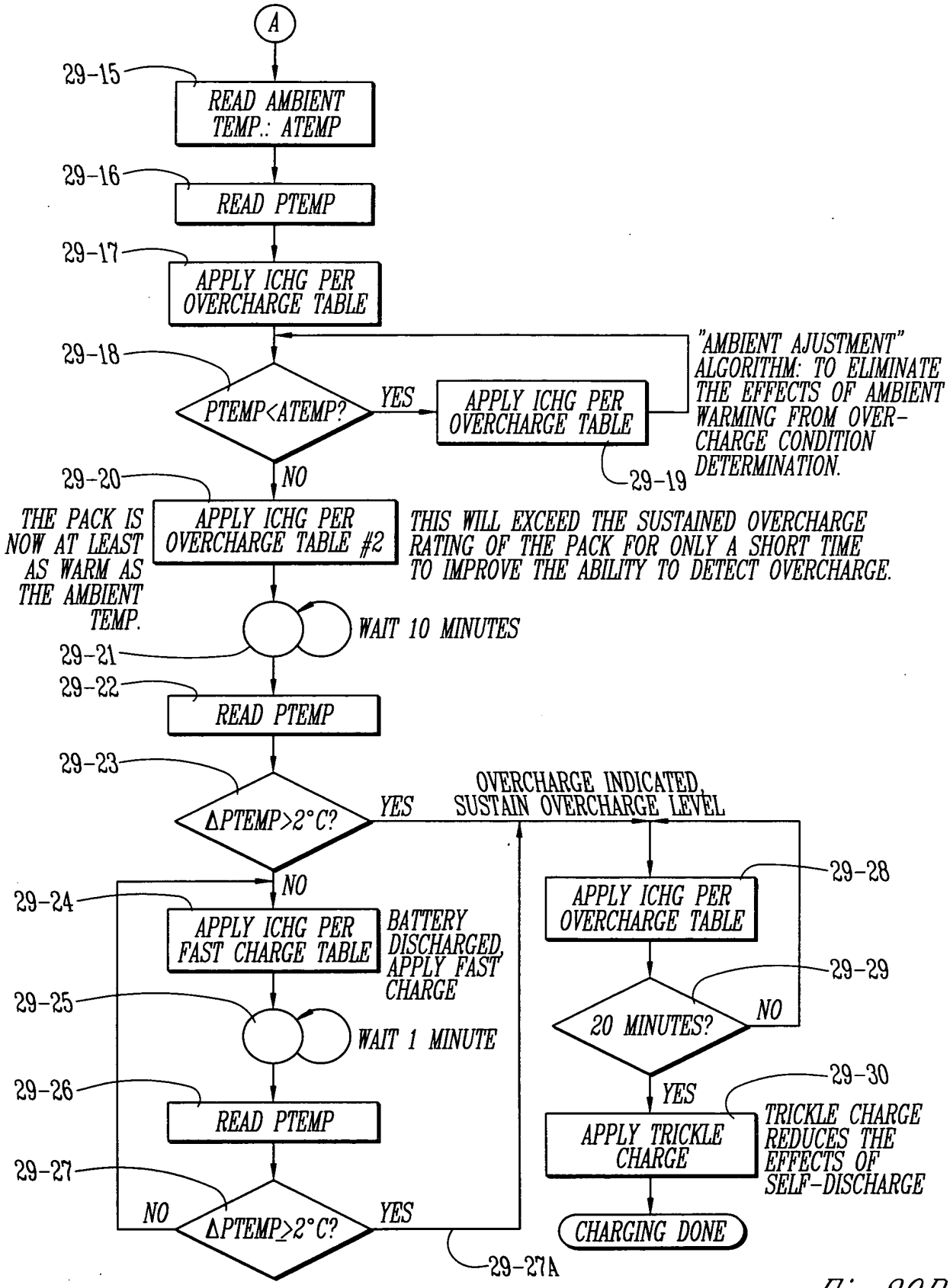

A
29-15
READ AMBIENT TEMP.: ATEMP
29-16
READ PTEMP
29-17
APPLY ICHG PER OVERCHARGE TABLE
29-18
PTEMP<ATEMP?
YES
APPLY ICHG PER OVERCHARGE TABLE
29-19
"AMBIENT AJUSTMENT" ALGORITHM: TO ELIMINATE THE EFFECTS OF AMBIENT WARMING FROM OVER-CHARGE CONDITION DETERMINATION.
NO
29-20
APPLY ICHG PER OVERCHARGE TABLE #2
THE PACK IS NOW AT LEAST AS WARM AS THE AMBIENT TEMP.
THIS WILL EXCEED THE SUSTAINED OVERCHARGE RATING OF THE PACK FOR ONLY A SHORT TIME TO IMPROVE THE ABILITY TO DETECT OVERCHARGE.
WAIT 10 MINUTES
29-21
29-22
READ PTEMP
29-23
ΔPTEMP>2°C?
YES
OVERCHARGE INDICATED, SUSTAIN OVERCHARGE LEVEL
NO
29-24
APPLY ICHG PER FAST CHARGE TABLE
BATTERY DISCHARGED, APPLY FAST CHARGE
29-25
WAIT 1 MINUTE
29-26
READ PTEMP
29-27
NO
ΔPTEMP≥2°C?
YES
29-27A
29-28
APPLY ICHG PER OVERCHARGE TABLE
29-29
20 MINUTES?
NO
YES
29-30
APPLY TRICKLE CHARGE
TRICKLE CHARGE REDUCES THE EFFECTS OF SELF-DISCHARGE
CHARGING DONE

Fig. 29B

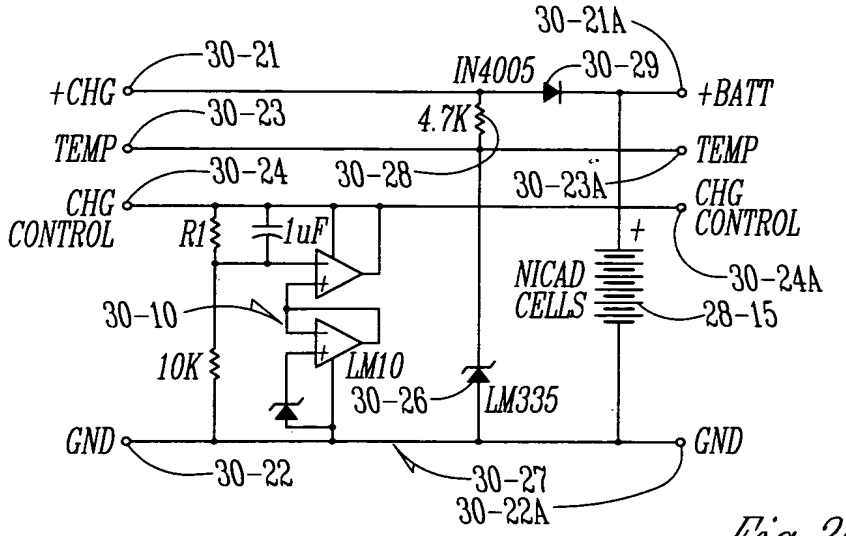

30-21A
30-21
IN4005
30-29
+CHG
+BATT
30-23
4.7K
TEMP
TEMP
30-24
30-28
30-23A
CHG
CONTROL
CHG
CONTROL
R1
1uF
+
NICAD
CELLS
30-24A
30-10
28-15
10K
LM10
30-26
LM335
GND
GND
30-22
30-27
30-22A

Fig. 30

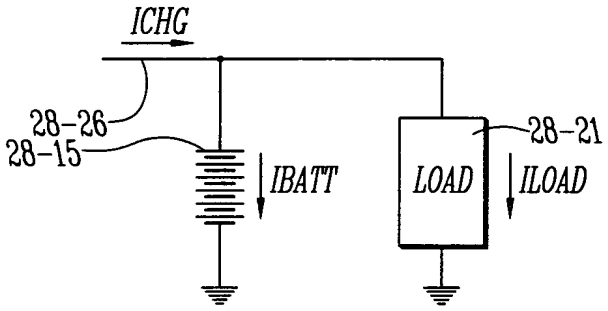

ICHG
28-26
28-15
IBATT
LOAD
28-21
ILOAD

Fig. 31

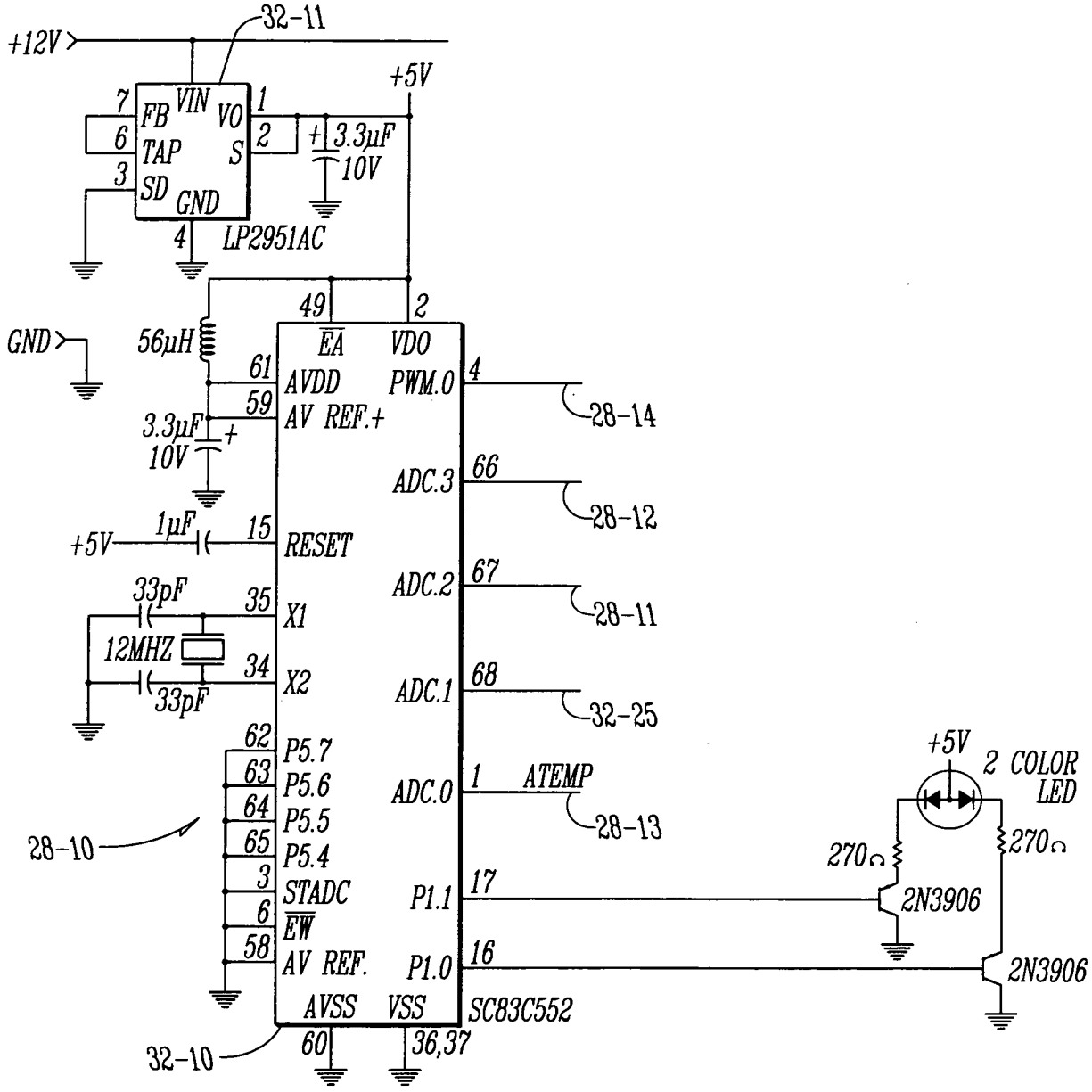

+12V
32-11
+5V
7 FB
6 TAP
3 SD
VIN
VO
S
GND
1
2
4
LP2951AC
3.3µF
10V
GND
56µH
49 EA
2 VDO
61 AVDD
59 AV REF.+
3.3µF
10V
4 PWM.0
28-14
ADC.3 66
28-12
+5V
1µF
15 RESET
ADC.2 67
28-11
33pF
35 X1
12MHZ
34 X2
33pF
ADC.1 68
32-25
62 P5.7
63 P5.6
64 P5.5
65 P5.4
3 STADC
6 EW
58 AV REF.
ADC.0 1 ATEMP
28-13
28-10
P1.1 17
P1.0 16
AVSS
VSS
SC83C552
32-10
60
36,37
+5V
2 COLOR LED
270Ω
270Ω
2N3906
2N3906

Fig. 32A

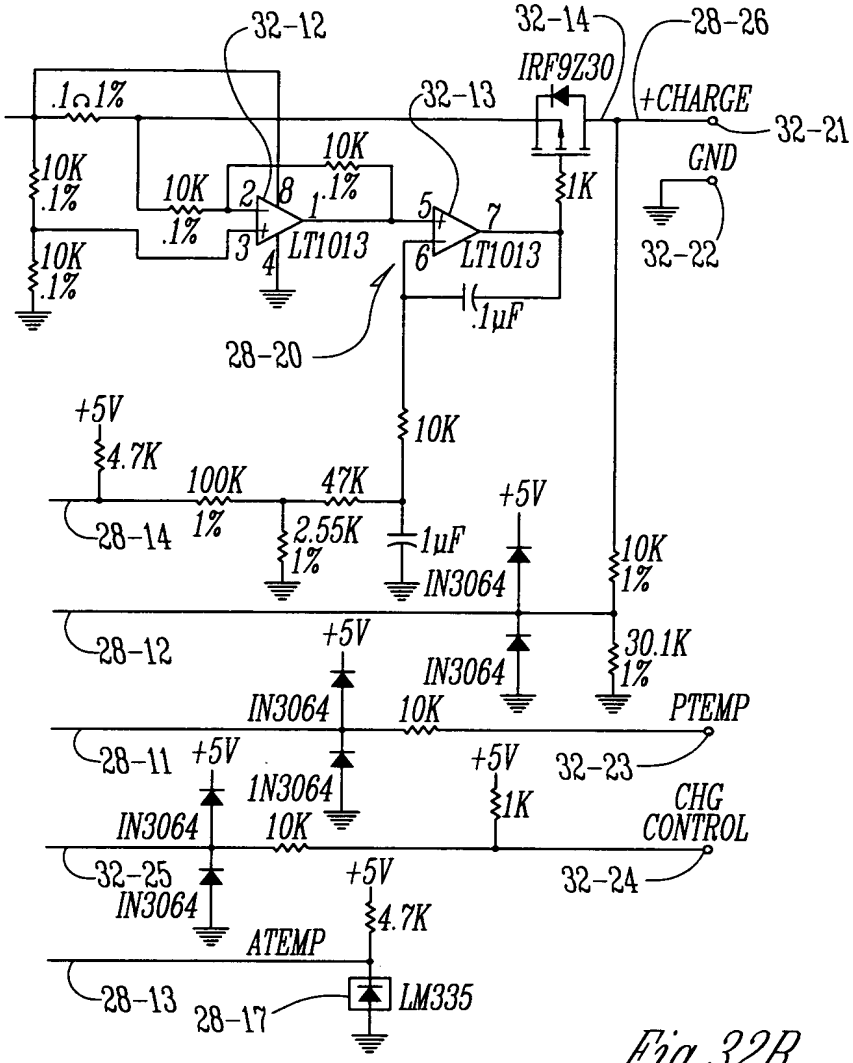

32-12
32-14
28-26
IRF9Z30
.1Ω 1%
32-13
+CHARGE
32-21
10K
.1%
10K
.1%
10K
.1%
10K
.1%
2
8
1
LT1013
3
4
5
7
6
LT1013
1K
GND
32-22
.1μF
28-20
+5V
4.7K
10K
100K
1%
47K
28-14
2.55K
1%
1μF
IN3064
+5V
10K
1%
28-12
+5V
IN3064
IN3064
10K
30.1K
1%
PTEMP
28-11
+5V
32-23
+5V
1N3064
1K
CHG
CONTROL
IN3064
10K
32-25
32-24
IN3064
+5V
4.7K
ATEMP
28-13
28-17
LM335

Fig. 32B

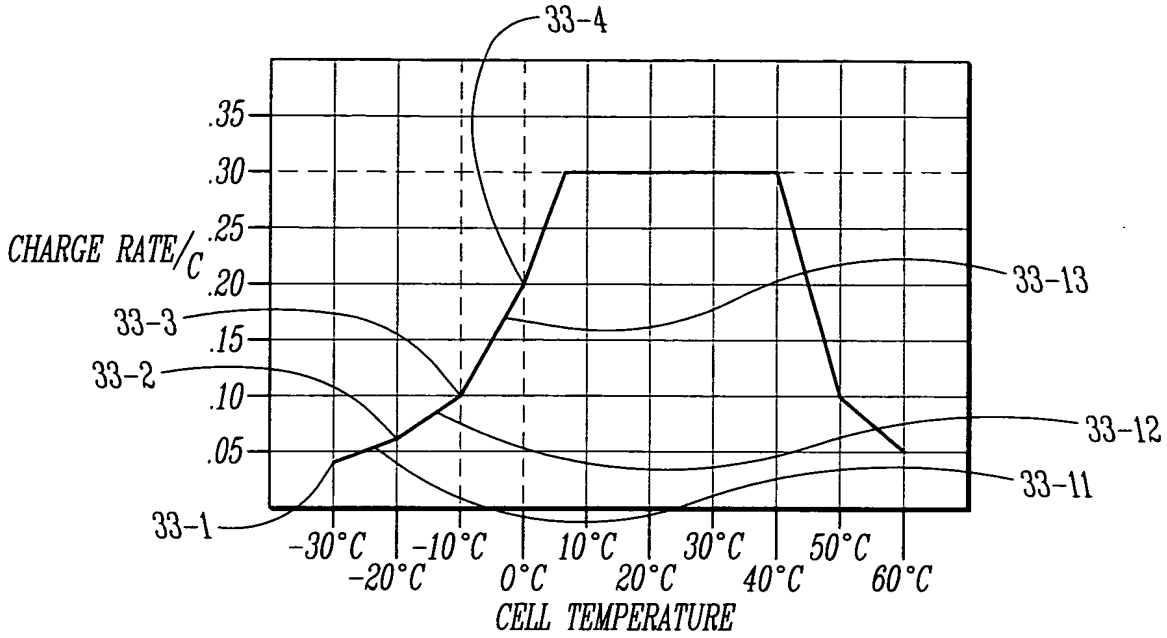

33-4
.35
.30
.25
.20
.15
.10
.05
CHARGE RATE/C
33-13
33-3
33-2
33-12
33-11
33-1
-30°C
-20°C
-10°C
0°C
10°C
20°C
30°C
40°C
50°C
60°C
CELL TEMPERATURE

Fig. 33

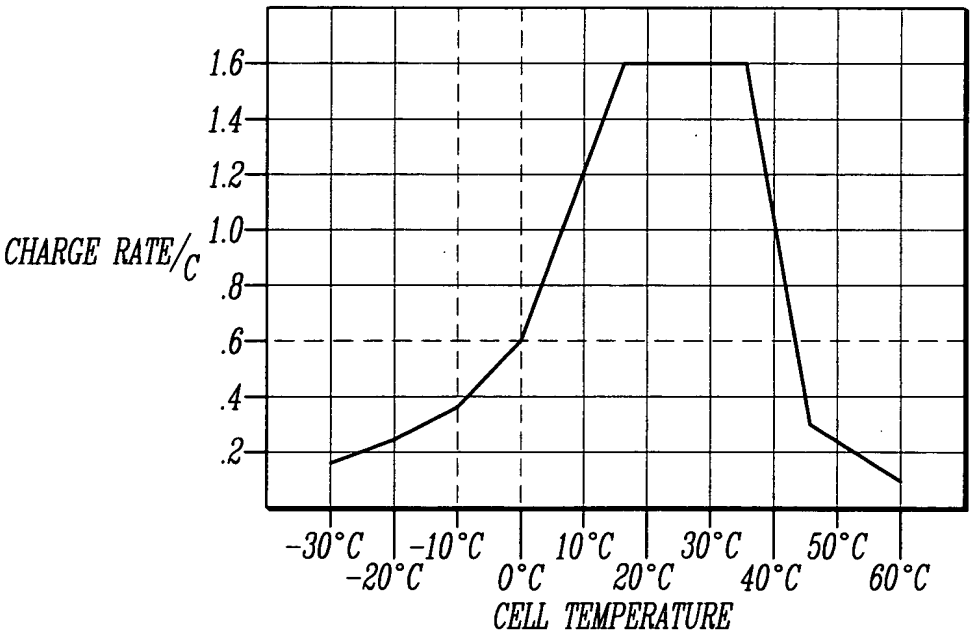
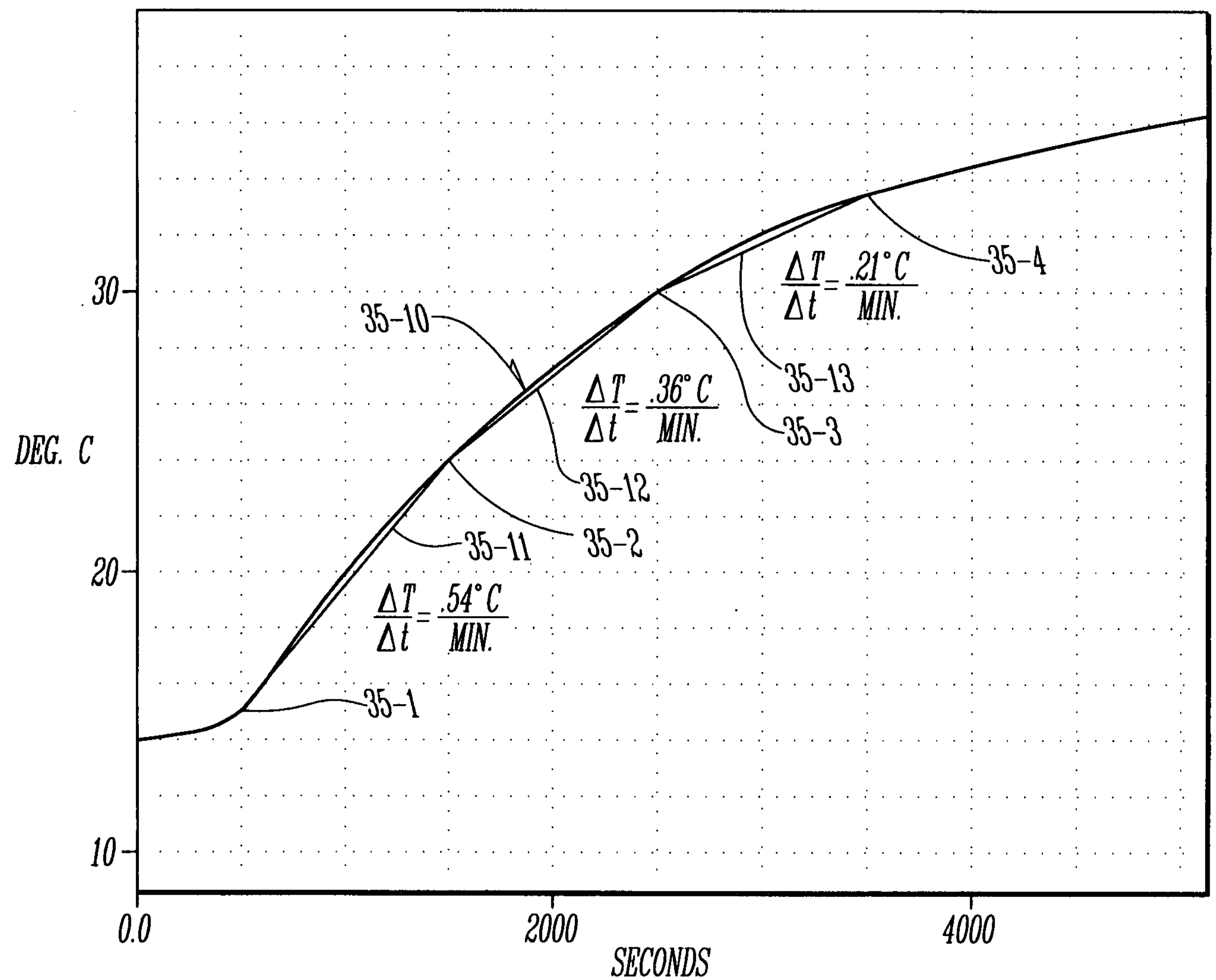

1.6
1.4
1.2
1.0
.8
.6
.4
.2
CHARGE RATE/C
-30°C
-20°C
-10°C
0°C
10°C
20°C
30°C
40°C
50°C
60°C
CELL TEMPERATURE

Fig. 34



DEG. C
30
20
10
0.0
2000
4000
SECONDS
35-1
35-2
35-3
35-4
35-10
35-11
35-12
35-13
$\frac{\Delta T}{\Delta t} = \frac{.54° C}{MIN.}$
$\frac{\Delta T}{\Delta t} = \frac{.36° C}{MIN.}$
$\frac{\Delta T}{\Delta t} = \frac{.21° C}{MIN.}$

Fig. 35

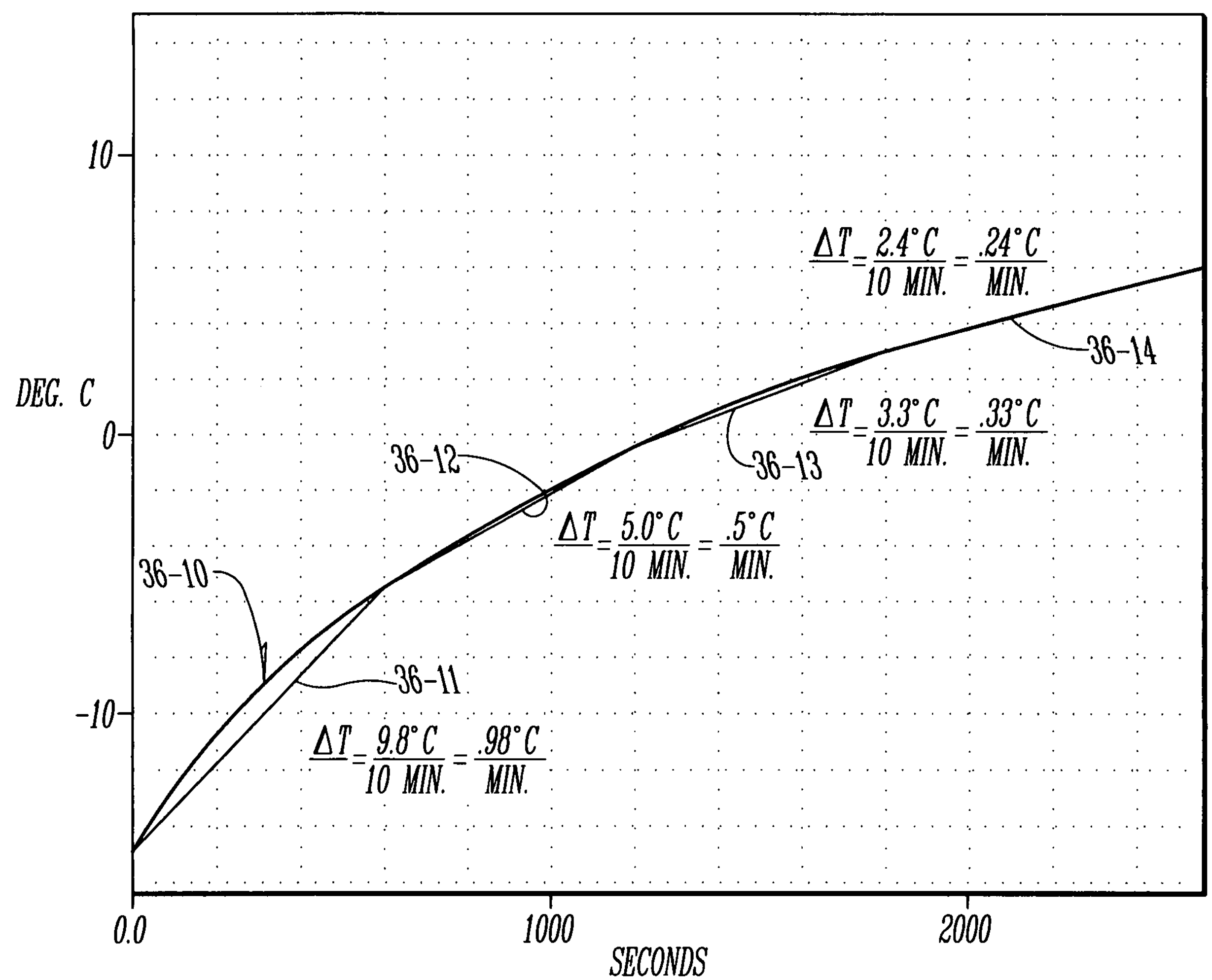


Fig. 36

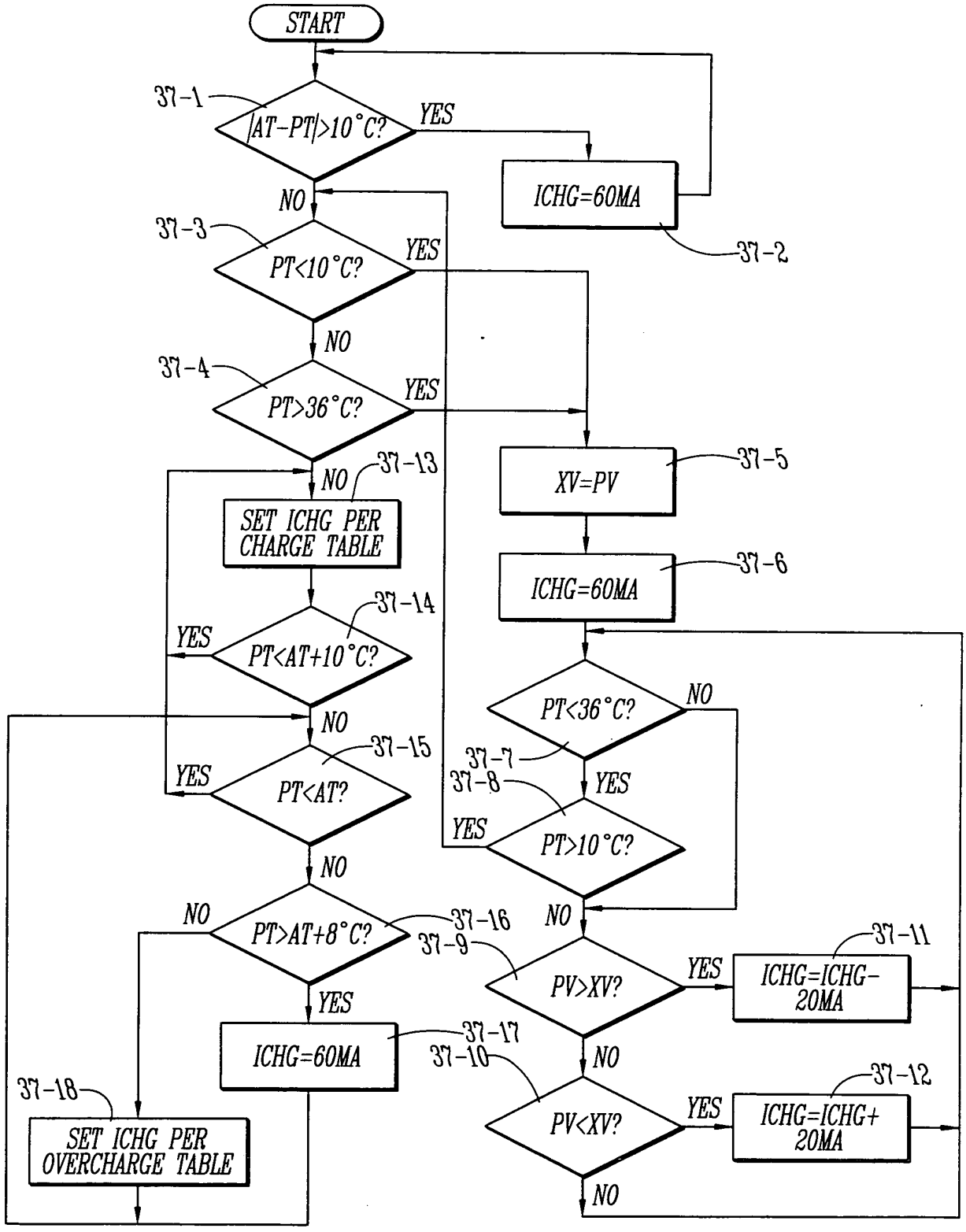

START
37-1
|AT-PT|>10°C?
YES
ICHG=60MA
37-2
NO
37-3
PT<10°C?
YES
NO
37-4
PT>36°C?
YES
37-5
XV=PV
37-6
ICHG=60MA
37-13
NO
SET ICHG PER CHARGE TABLE
37-14
YES
PT<AT+10°C?
NO
37-15
YES
PT<AT?
NO
37-16
NO
PT>AT+8°C?
YES
37-17
ICHG=60MA
37-18
SET ICHG PER OVERCHARGE TABLE
NO
37-7
PT<36°C?
37-8
YES
PT>10°C?
YES
NO
37-9
PV>XV?
YES
37-11
ICHG=ICHG-20MA
NO
37-10
PV<XV?
YES
37-12
ICHG=ICHG+20MA
NO

Fig. 37

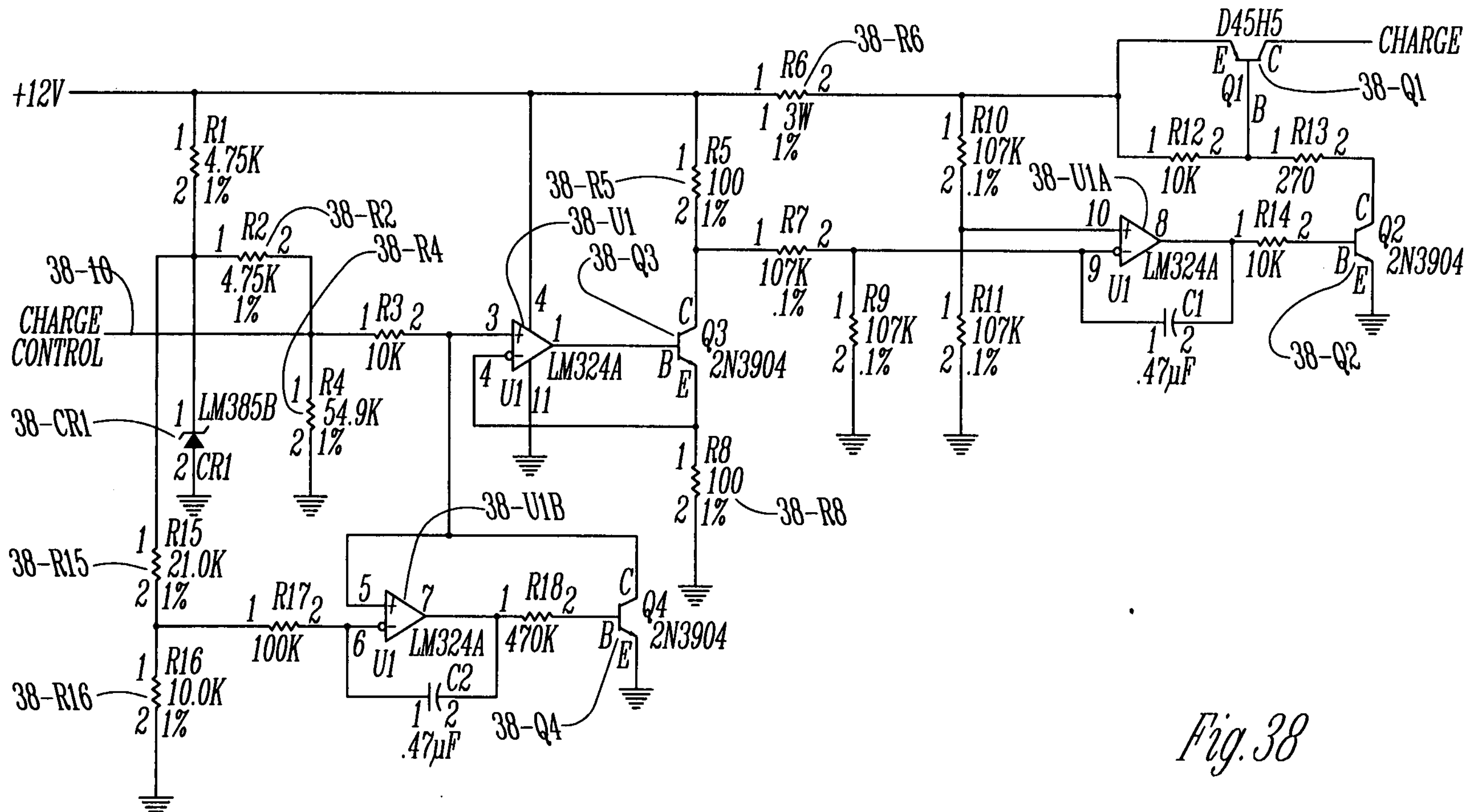

+12V
R1
4.75K
1%
R2
4.75K
1%
38-R2
38-R4
38-10
CHARGE
CONTROL
R3
10K
R4
54.9K
1%
LM385B
CR1
38-CR1
R15
21.0K
1%
38-R15
R16
10.0K
1%
38-R16
R17
100K
38-U1B
U1
LM324A
C2
.47μF
R18
470K
Q4
2N3904
38-Q4
38-U1
38-Q3
LM324A
U1
Q3
2N3904
38-R5
R5
100
1%
R6
3W
1%
38-R6
R7
107K
.1%
R8
100
1%
38-R8
R9
107K
.1%
R10
107K
.1%
R11
107K
.1%
38-U1A
U1
LM324A
C1
.47μF
D45H5
Q1
CHARGE
38-Q1
R12
10K
R13
270
R14
10K
Q2
2N3904
38-Q2

Fig. 38

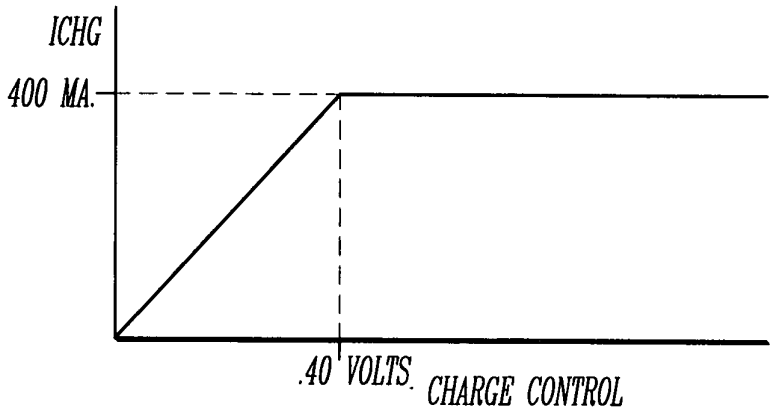


Fig. 39

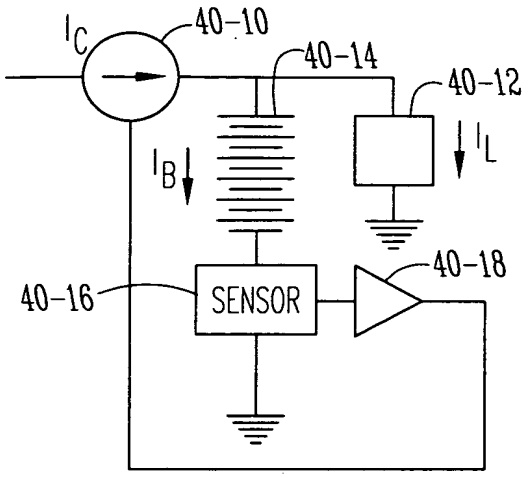


Fig. 40

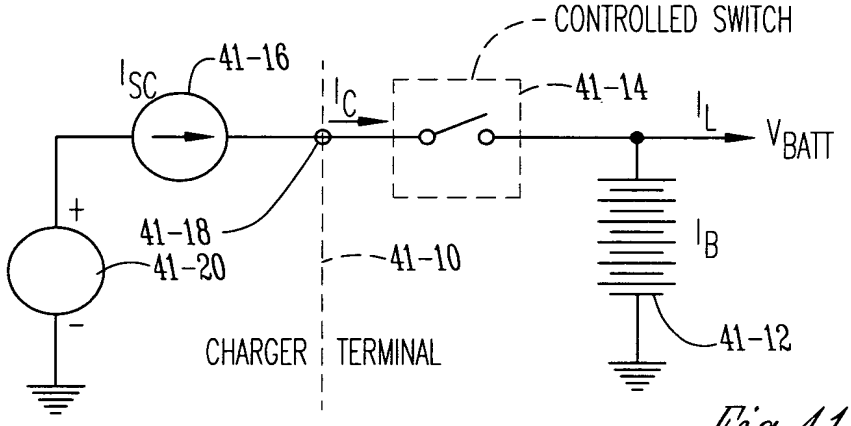


Fig. 41

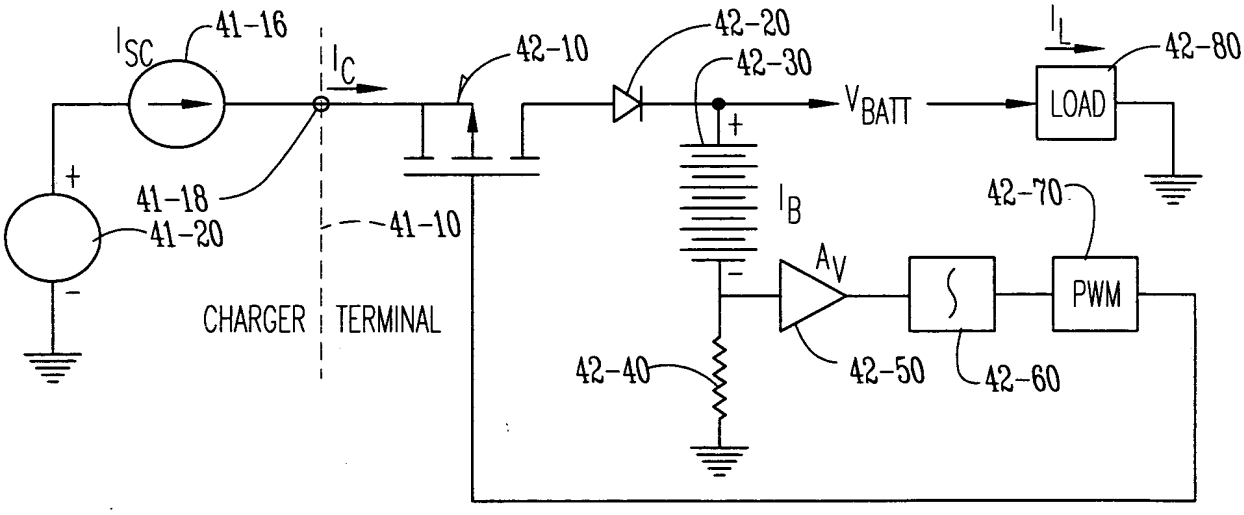


Fig. 42

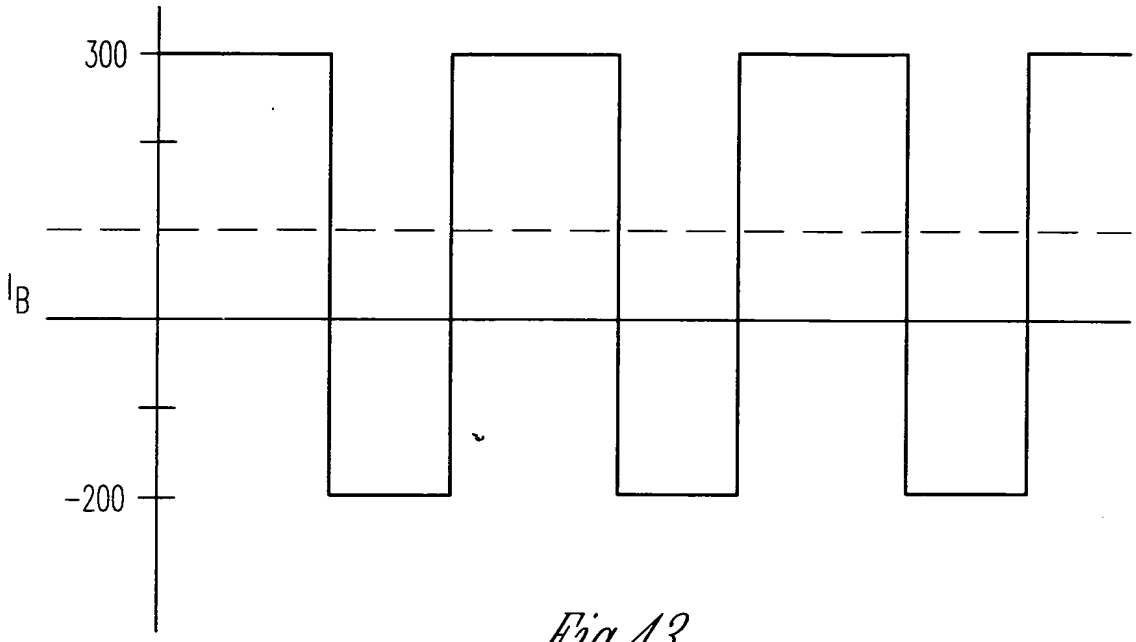


Fig. 43

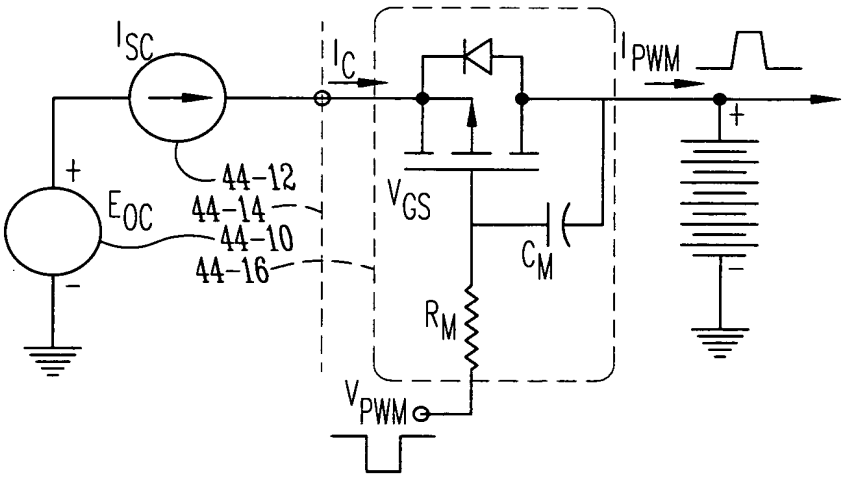
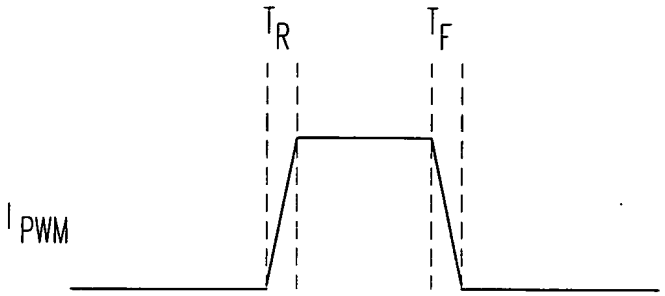


Fig. 44



T_R, ≈ .1 RC
T_F

Fig. 45

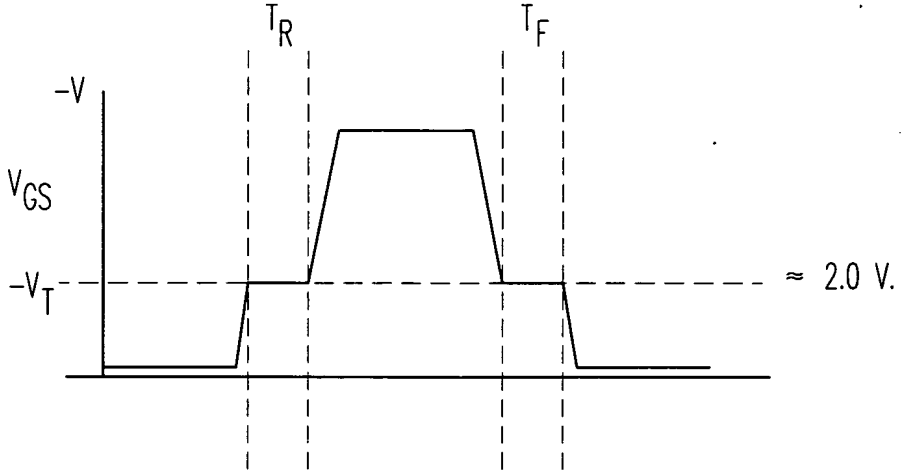


Fig. 46